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THESIS

ANALYSIS OF VOLTAGE AND CURRENT SIGNAL PROCESSING IN A LI-ION BATTERY MANAGEMENT SYSTEM

by

Jerome Sean McConnon

September 2010

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Giovanna Oriti

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13. ABSTRACT (maximum 200 words)

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Based on the BMS's successful operation, the processing of voltage and current signals in the BMS is researched and documented in this thesis. The documentation is provided through a thorough signal analysis before and after each component. Specifically, the current signal is analyzed and the processes of a Hall Effect Sensor, an instrument amplifier, and an analog-to-digital converter are described. Additionally, the voltage signal and its processing by a voltage-to-frequency converter are analyzed and the FPGA programming is described. The accuracy of the collected data is shown and possible improvements to the system are documented.

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ANALYSIS OF VOLTAGE AND CURRENT SIGNAL PROCESSING IN A LI-ION BATTERY MANAGEMENT SYSTEM

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requirements for the degree of

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ABSTRACT

The Naval Postgraduate School's Battery Management System (BMS) manages Li-ion batteries in a possible storage system for pulsed power weapons aboard Naval Vessels. The system charges the batteries with a buck converter according to the Constant Current Constant Voltage method. The BMS uses analog equipment to measure signals and then digitally converts signals for transmittal to a Field Programmable Gate Array (FPGA). Software processing controls the voltage and current directed to the batteries to maintain proper control and maintenance of the batteries.

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LIST OF ACRONYMS AND ABBREVIATIONS

A/D	Analog-to-Digital
AC	Alternating Current
ADC	Analog-to-Digital Converter
BMS	Battery Management System
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
FPGA	Field Programmable Gate Array
LCS	Littoral Combat Ship
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OPAMP	Operational Amplifier
PCB	Printed Circuit Board
PI	Proportional Integrator

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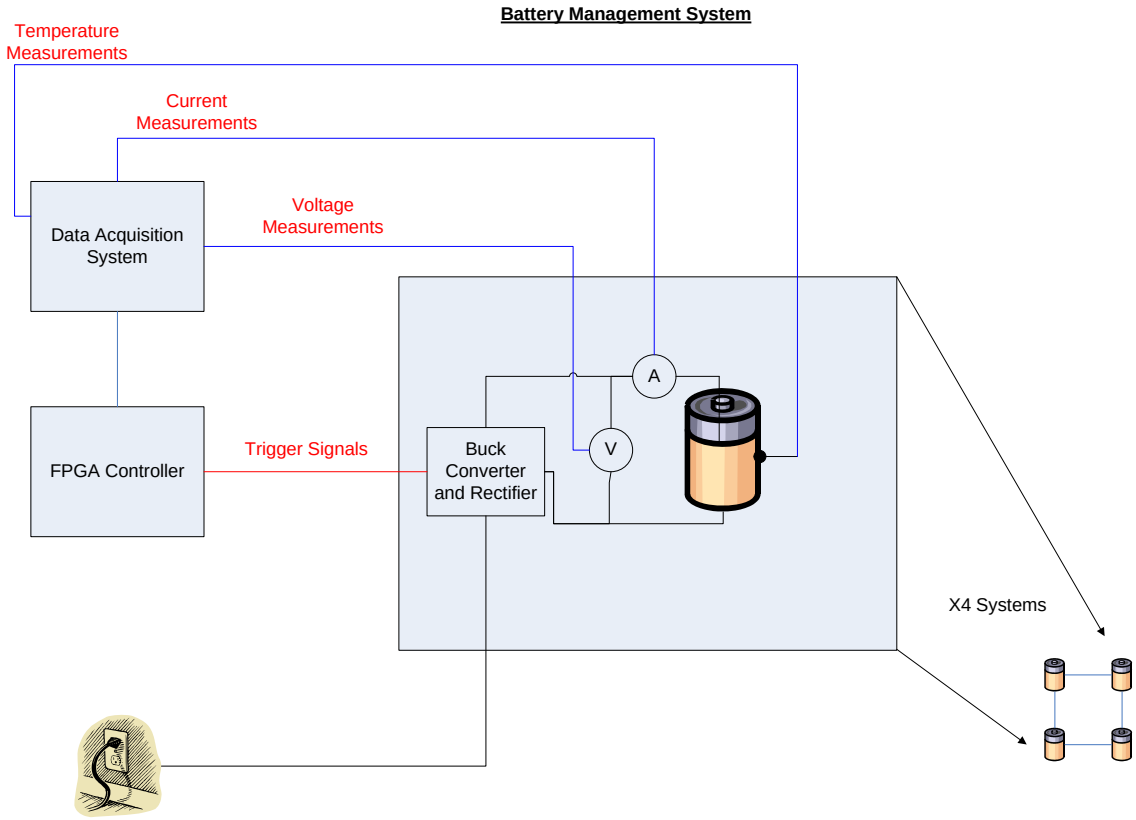
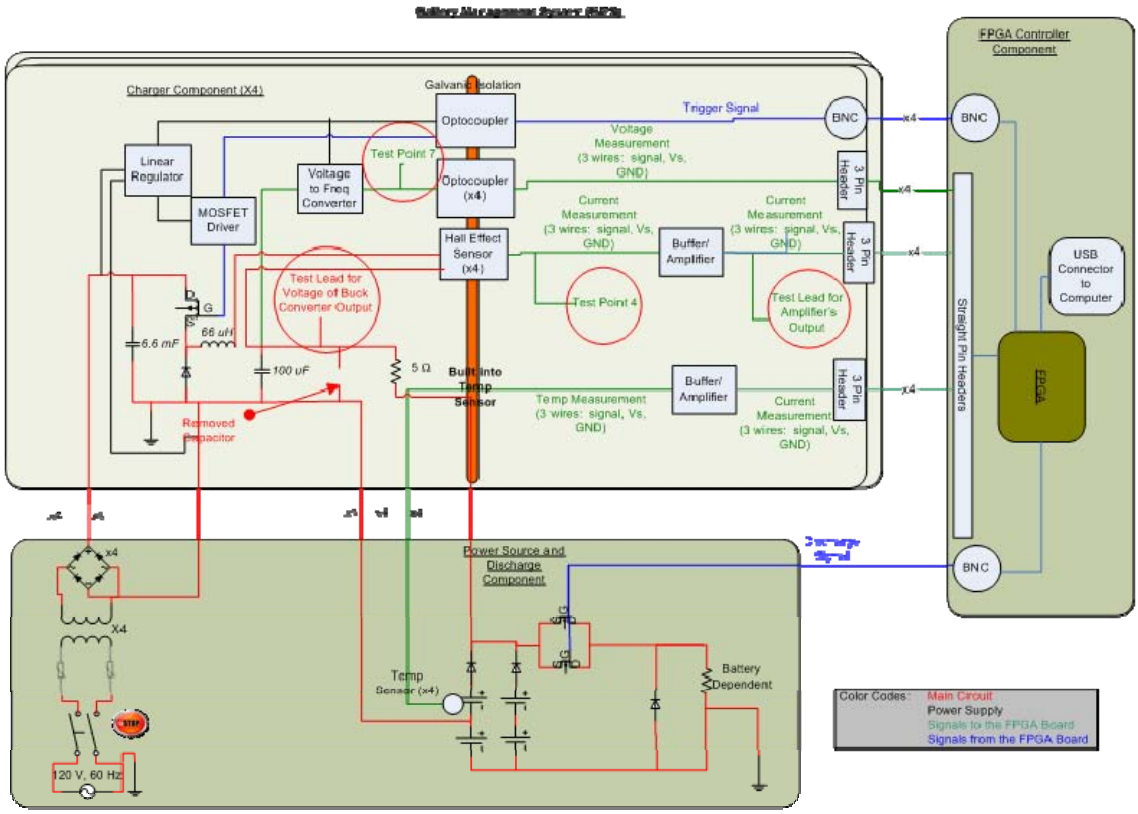
EXECUTIVE SUMMARY

The analysis of the signal processing techniques used in the Battery Management System (BMS) at the Naval Postgraduate School is presented in this thesis. The BMS's design can manage the charge and discharge of four Li-ion batteries. The discharge simulates the rapid power consumption by a pulsed power supply. The following figure is a functional representation of the BMS.



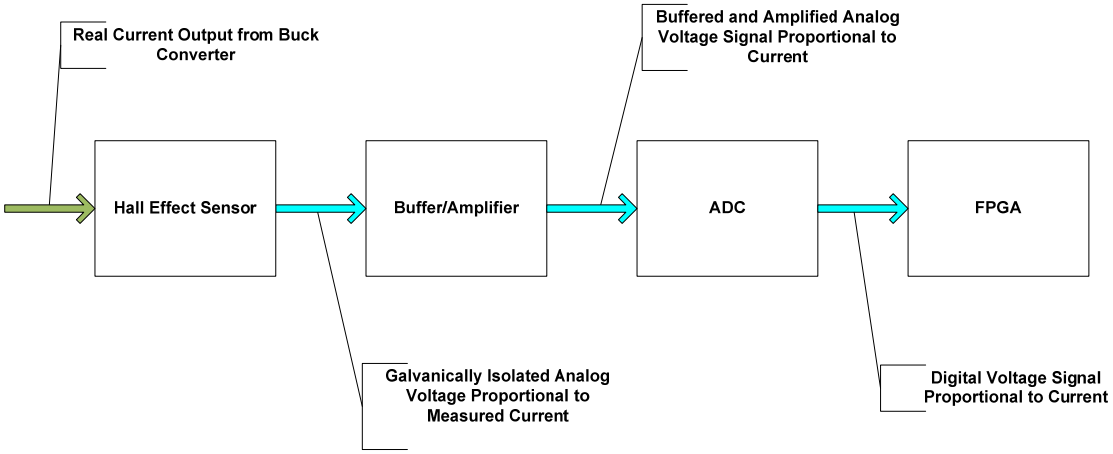
Functional Diagram of the BMS

At its core, the BMS is made of four Field Programmable Gate Array (FPGA) controlled buck converters. There is one converter for each battery. Additionally, each converter contains sensors and a control system to allow for digital control of the buck converter by the FPGA. The FPGA varies the buck converter's duty cycle to control the battery current. The details of the BMS are shown below.



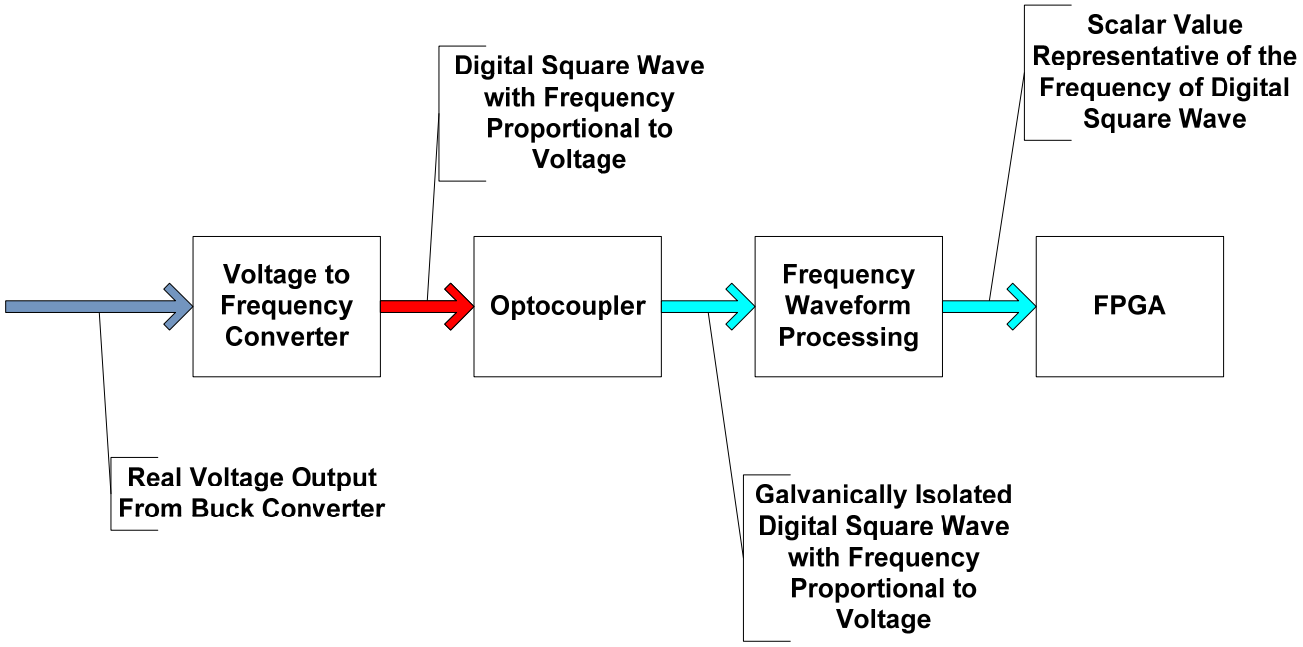
Battery Management System Components

The current and voltage signals that the BMS measures and processes are the exclusive concern of this thesis. The components that handle the current signal are a Hall Effect Sensor, a buffer/amplifier, an Analog-to-Digital Converter (ADC), and the FPGA. The following block diagram shows how these components are related.



Current Signal Flow Path

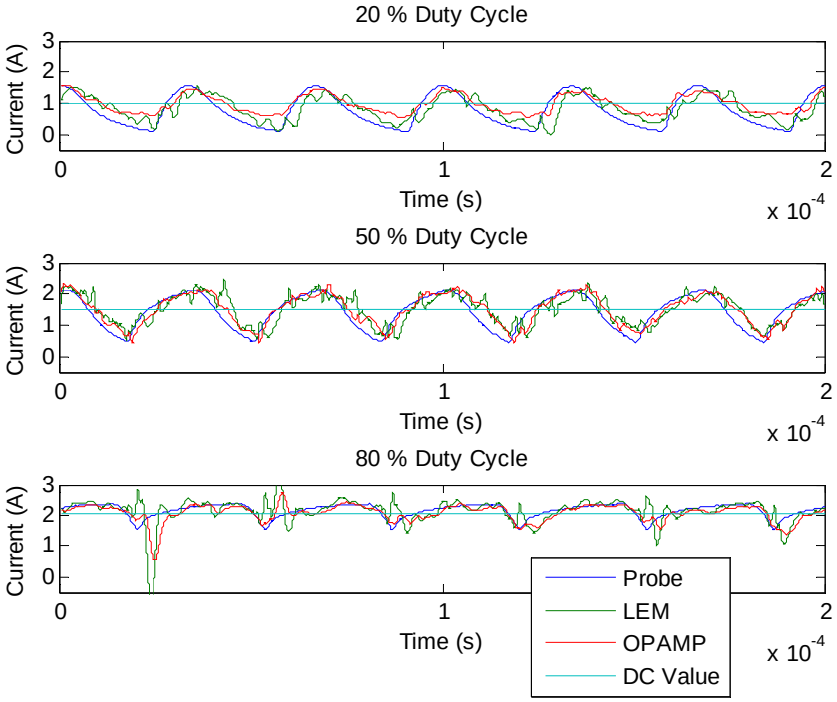
The components that handle the voltage signal are the Voltage-to-Frequency converter, an optocoupler for galvanic isolation, a SIMULINK® model for processing the output from the Voltage-to-Frequency converter, and the FPGA.



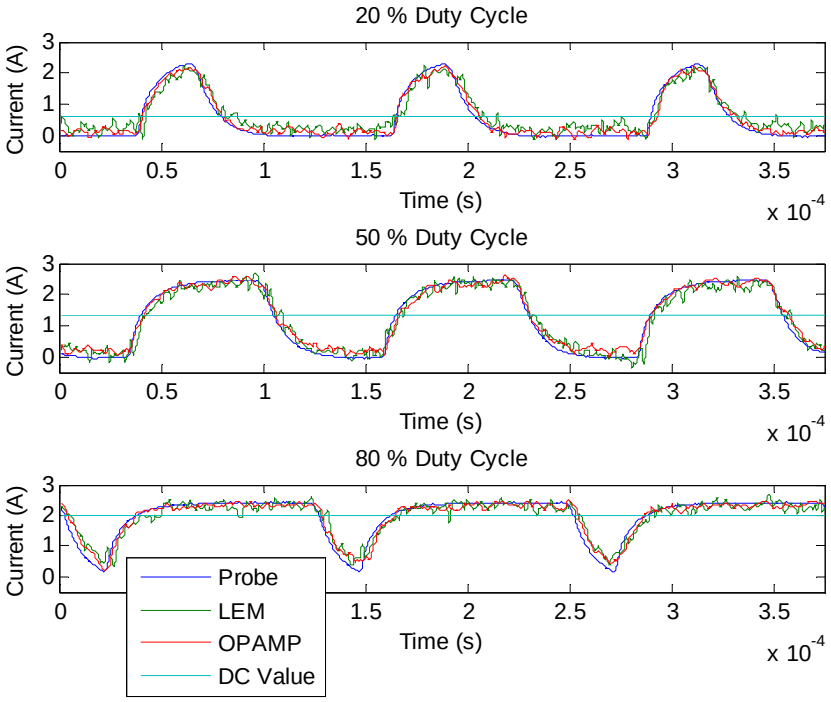
Voltage Signal Flow Path

The goal of this thesis is to analyze how each block in the above two figures affects the signal and document those effects.

For the current signal, two sets of data were collected for analysis. One set with the buck converter operating at 30 kHz, and the other set at 8 kHz. For each frequency, testing included measurements at 20%, 50%, and 80% duty cycles. The results of the testing are below.



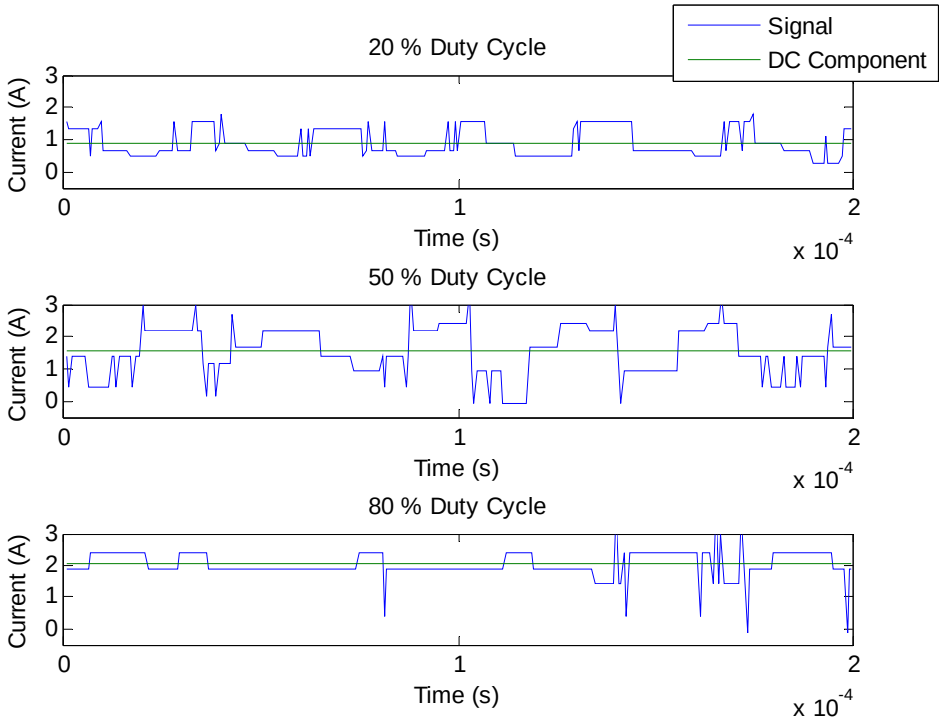
30 kHz Test Results. DC Value is the DC Component of OPAMP Signal



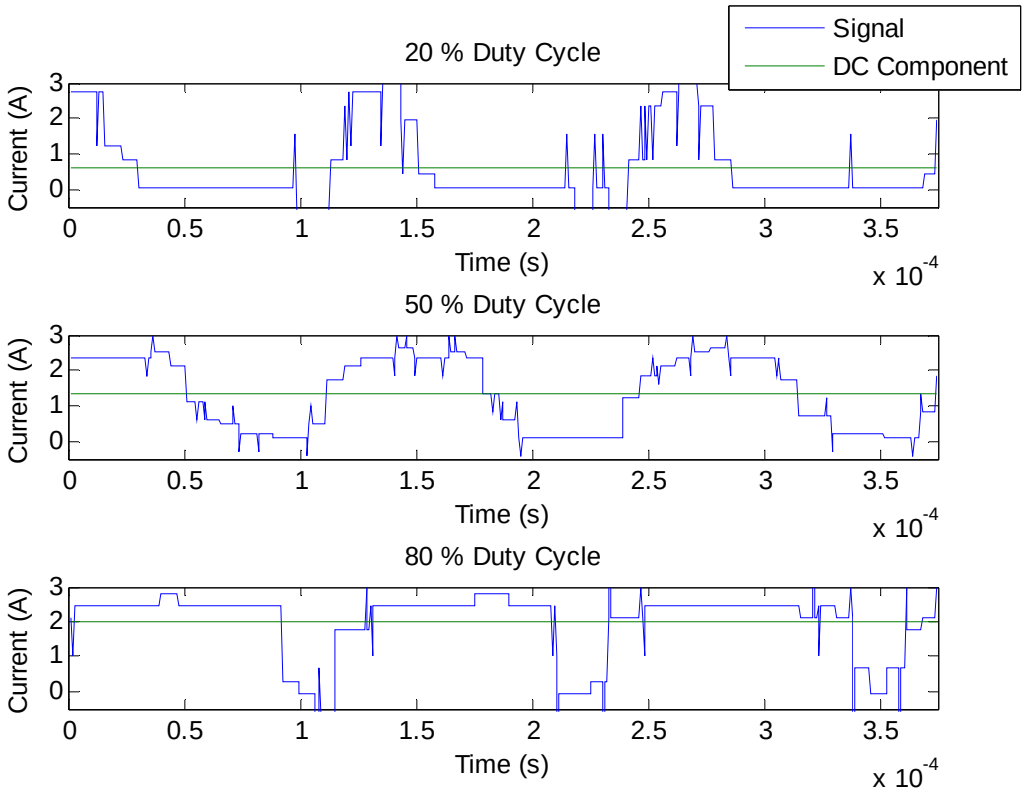
8 kHz Test Results. DC Value is the DC Component of OPAMP Signal

The figures above show that the signal's original waveform is well preserved through the analog sensor process.

The BMS software includes the ability to display the signal that the FPGA receives and works with. This data is shown below.



Digital Waveforms in FGPA. 30 kHz Signal.



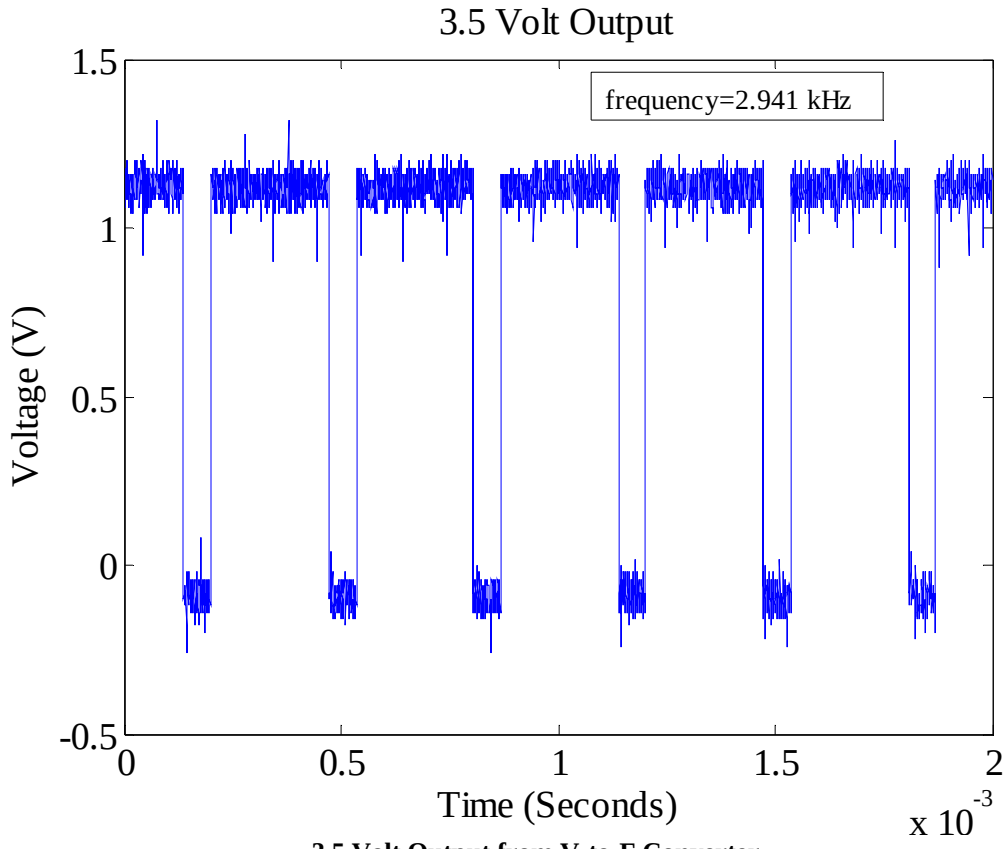
Digital Waveforms in FGPA. 8 kHz Signal.

The digital waveforms are significantly distorted in shape from the analog input. Despite this distortion, the DC component of the signal is only slightly disturbed.

The proportional integrator controller of the buck converter corrects the waveform distortion. The controller integrates the signal twice before processing. This smoothes out the signals and extracts the intact DC value of the signals. As the DC component of current is what charges the battery, this processing is appropriate. Therefore, even though the digital conversion introduces significant error, the FPGA does not see the error and uses only the correct DC values for processing.

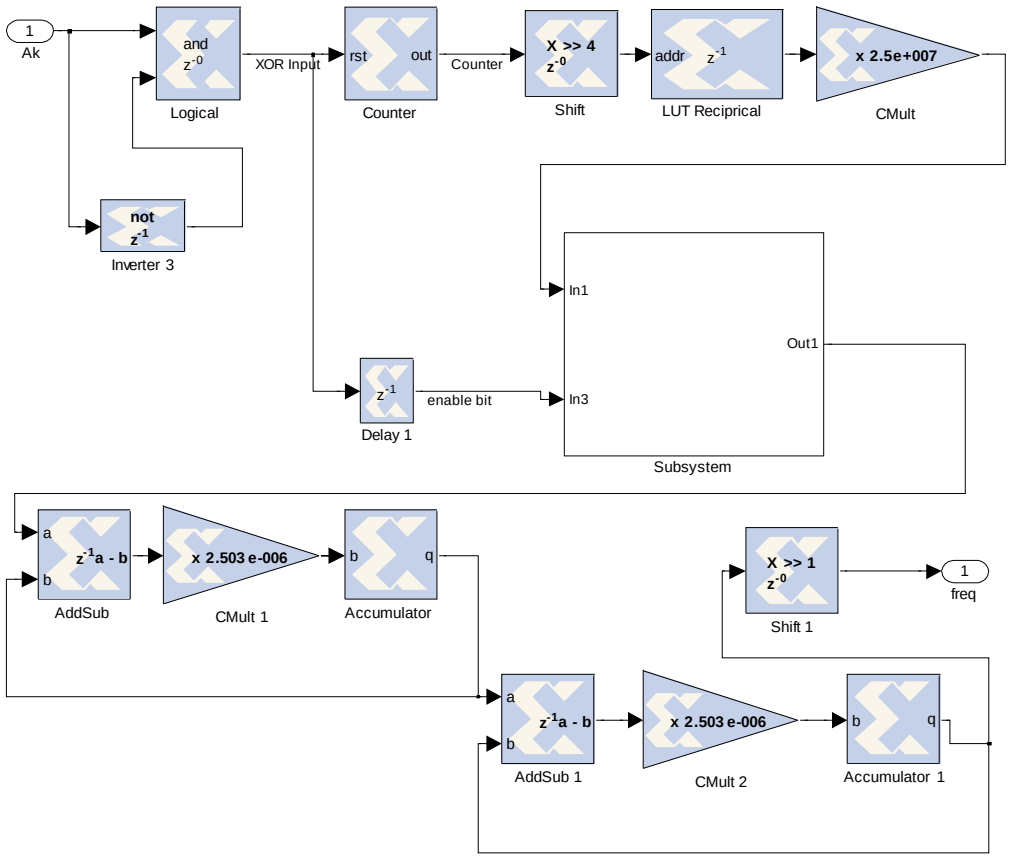
The voltage signal processing method is less complicated, as the signal is converted digitally when the Voltage to Frequency converter measures it. The converter's output is a digital square wave with frequency proportional to the voltage. The datasheet for the converter includes a conversion factor, but it is not accurate in this application.

The converter requires calibration to ensure proper scaling and offset prior to operation. The figure below contains the results of a calibrated 3.5 Volt signal.



3.5 Volt Output from V-to-F Converter.

This waveform, although digital, is not suitable for use in the FPGA. The FPGA requires a value that equals the frequency of the waveform. To accomplish this, Professor Alex Julian of the Naval Postgraduate School created a SIMULINK® model that is shown below.



SIMULINK® Model to Process Frequency Waveform

The model is very accurate with error in frequency that is less than 3%. This corresponds to a less than 1% error in measured voltage.

The BMS functions well for its designed purpose. It allows for digital, automatic management of Li-ion batteries. This technology is a necessary tool in order to move towards highly automated, minimally manned naval vessels.

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I. INTRODUCTION

A. BACKGROUND

The Navy is actively researching technology for the development of integrated electric ships. These ships have a major advantage over conventionally powered ships in their efficiency. Ships in use today require two prime movers for operation. Depending on the power source of the ship, gasoline or steam powers these prime movers. In either case, one prime mover provides power to propulsion and another creates electricity to power the ship's systems. Further, for greatest efficiency, the prime movers operate at 1000's of RPM. The propeller spins at a much slower rate, which means reduction gears are necessary in a mechanical drive system. A representation of a typical ship's drive structure is shown in Figure 1.

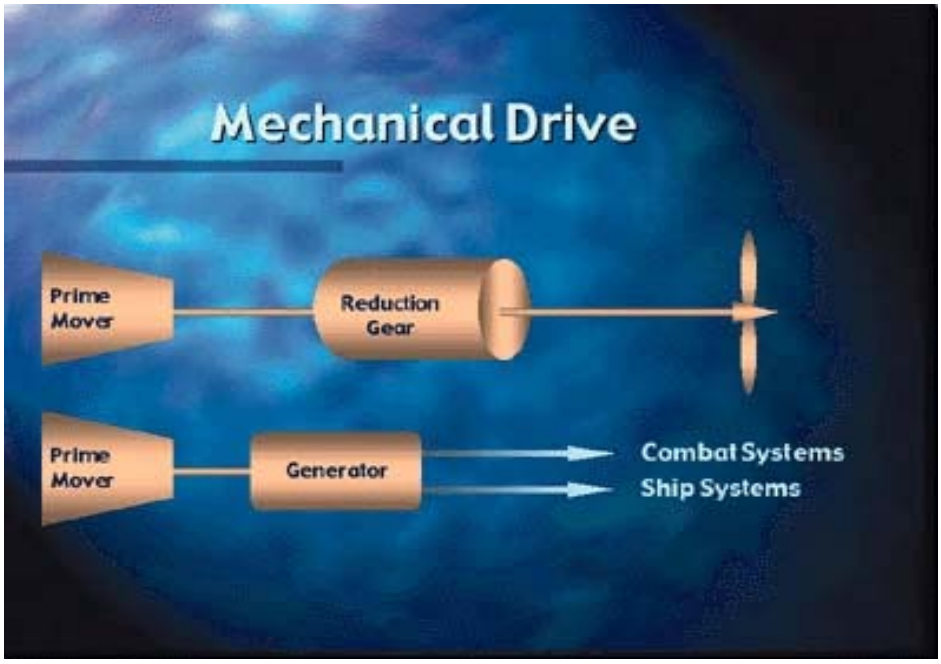

Figure 1. Mechanical Ship. From [1].

In contrast, an integrated electric ship's power system, shown in Figure 2, uses only one prime mover for both the propulsion and the ship's electrical needs. The prime mover still spins at a high speed, but only powers the generator. The motor drive converts the electrical output to a form usable by the propulsion motor. Since this conversion is electrical, not mechanical, reduction gears are not necessary.

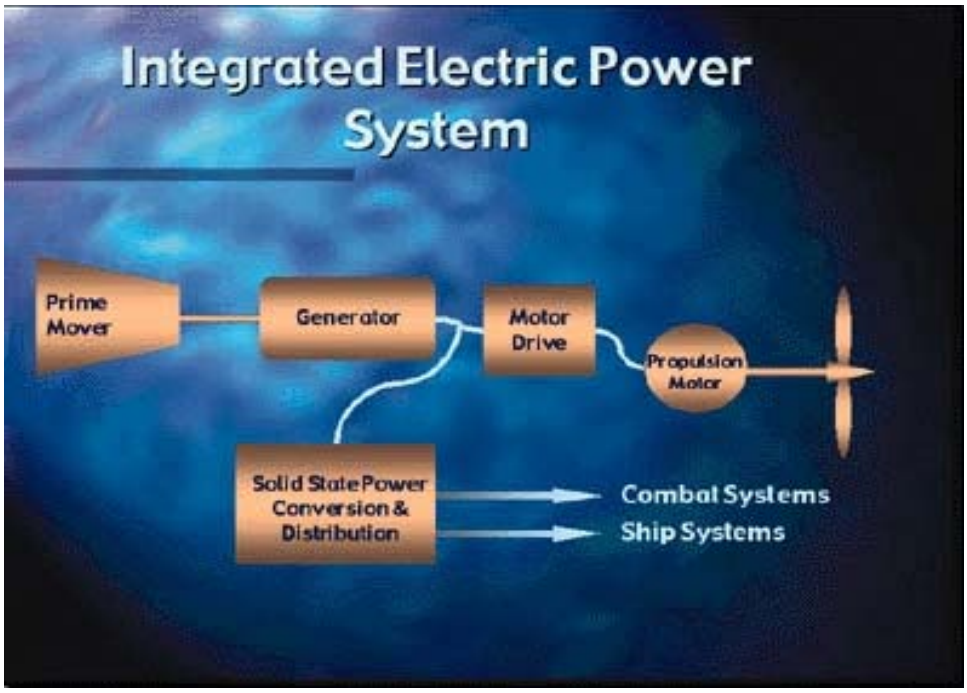

Figure 2. Integrated Electric Ship. From [1].

The removal of a prime mover and reduction gears removes two sources of mechanical energy loss in the system. However, this is not the largest source of energy savings. The major energy savings comes from the energy flexibility of an integrated electric ship. In a mechanical drive ship, 75%-85% of the power produced by the prime movers is dedicated to propulsion [2]. This power cannot be routed elsewhere, even when the propulsion system is operating at less than full capacity. In contrast, an integrated electric ship can deliver power to anywhere on the ship, including electrical energy based weapons.

This energy diversion can occur very quickly. Therefore, if a ship is traveling at high speed and suddenly needs to use an electrical weapon, the ship can momentarily divert power to the weapons system, while only slightly losing speed. This is a much more efficient use of the available energy onboard Naval Vessels. Current estimates expect a 15%–19% fuel savings over a similar mechanical drive ship due to this flexibility [2].

The advent of integrated electric ships is in conjunction with the development of pulsed power weapons systems. Pulsed power weapon systems require large amounts of energy in a very short period of time. Li-ion batteries have the power rating and energy storage ratings necessary to power such weapon systems [3].

The purpose of the BMS at the Naval Postgraduate School is to further research into energy storage for use in pulsed power weapons systems onboard Naval Vessels. The BMS is a small-scale model of what would be used onboard Naval Vessels. The BMS is pictured in Figure 3.

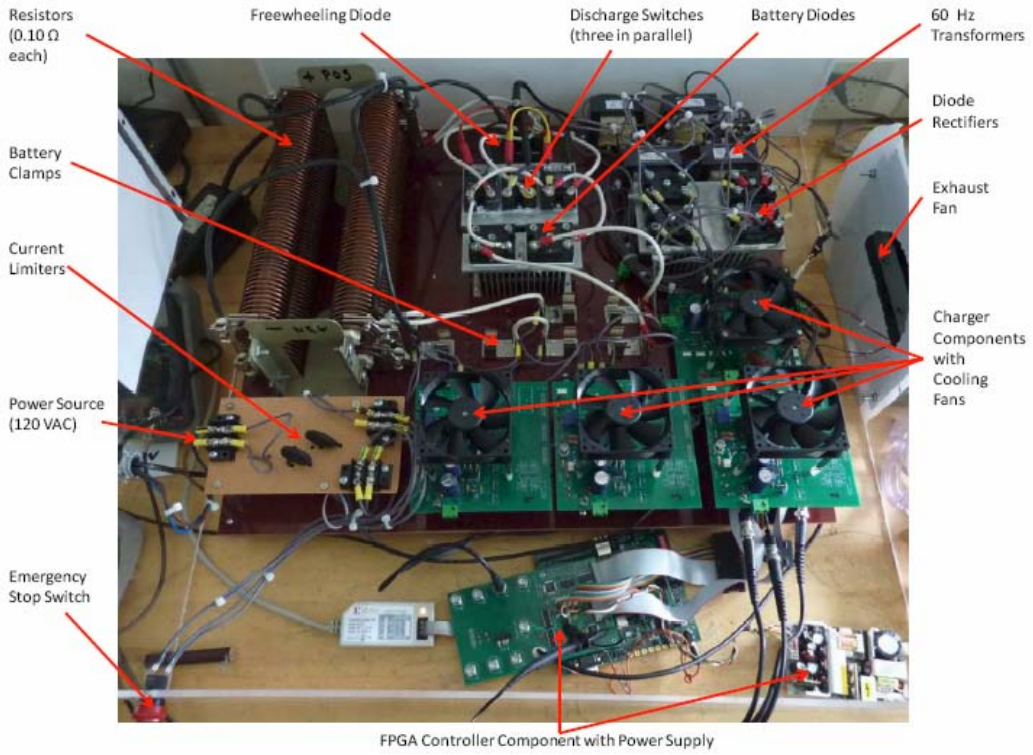

Figure 3. Assembled BMS. From [3].

Through its digital control structure, the BMS allows automatic management of Li-ion batteries. Proper management is critical as Li-ion batteries can fail catastrophically if improperly handled. This automated system is an example of one of many required technologies key to the success of the Navy's next generation LCS vessels.

The manning onboard LCS 1 and 2 are significantly lower than other Navy ships of similar size. This is possible due to the high level of automation that exists onboard the ships. LCS 1, which got underway on its first operational deployment on February 10, 2010, had a core crew of 40 Officers and Sailors [4]. Due to the advanced technology required for an Integrated Electric Drive ship, it is likely that such a ship would also have high levels of automation and minimal manning. A system like the BMS would be required for a ship armed with a pulsed power weapons system.

Major Frank Filler constructed the BMS as part of his thesis presented in September 2009 [3]. The BMS is currently partially complete; it can charge and discharge one battery. When operational, the BMS will control four batteries simultaneously. The BMS dedicates a PCB with the buck converter, voltage sensor, temperature sensor and current sensor to each battery. Currently card 1 is functional and controls a battery in slot 1. The work of this thesis is relevant to every PCB but is specifically applicable only to card 3. This is an important fact due to each card having unique voltage and current sensor systems. Each sensor has slightly different gains and offsets. The processing of data from each card needs to take into account the variables associated with each card to accurately control the batteries' charging and discharging rates.

B. THESIS GOALS

This thesis' first goal is to fully document the processing of current and voltage signals in the BMS and verify the accuracy of signal collection and processing. The second goal is to identify any changes that would improve the BMS operation.

C. THESIS ORGANIZATION

- Background information about integrated electric ships, their advantages and the role of Li-ion batteries is provided in Chapter I.
- The BMS and the individual components that are relative to this thesis is described in Chapter II.
- Information about the testing circuit and procedure to collect data is provided in Chapter III.
- The results of the testing documented in Chapter III are contained in Chapter IV.
- The thesis conclusion and suggestions for future work is given in Chapter V.

D. CHAPTER SUMMARY

The BMS plays a valuable role in pushing technology to enable the paradigm shift of Navy ships that leadership is currently seeking. Highly automated, minimally manned ships with Integrated Electric Drives could offer significant long-term savings in personnel costs, fuel, and construction.

The work presented here provides thorough documentation of the BMS signal processing and presents solutions to improve its operation.

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II. SYSTEM SUMMARY

A. INTRODUCTION

The BMS is a complex system with many components that work together to accomplish its goal to manage Li-ion batteries. In order to control the charge delivered to Li-Ion batteries, the cell current and voltage must be closely monitored. These two sensors are critical components of the BMS operation. This chapter will examine the components of the BMS that are applicable to the work of this thesis.

B. BMS

The BMS system consists of a transformer rectifier, a buck converter, an FPGA controller, a data acquisition system, and Li-ion batteries. The layout of these components is shown in Figure 4.

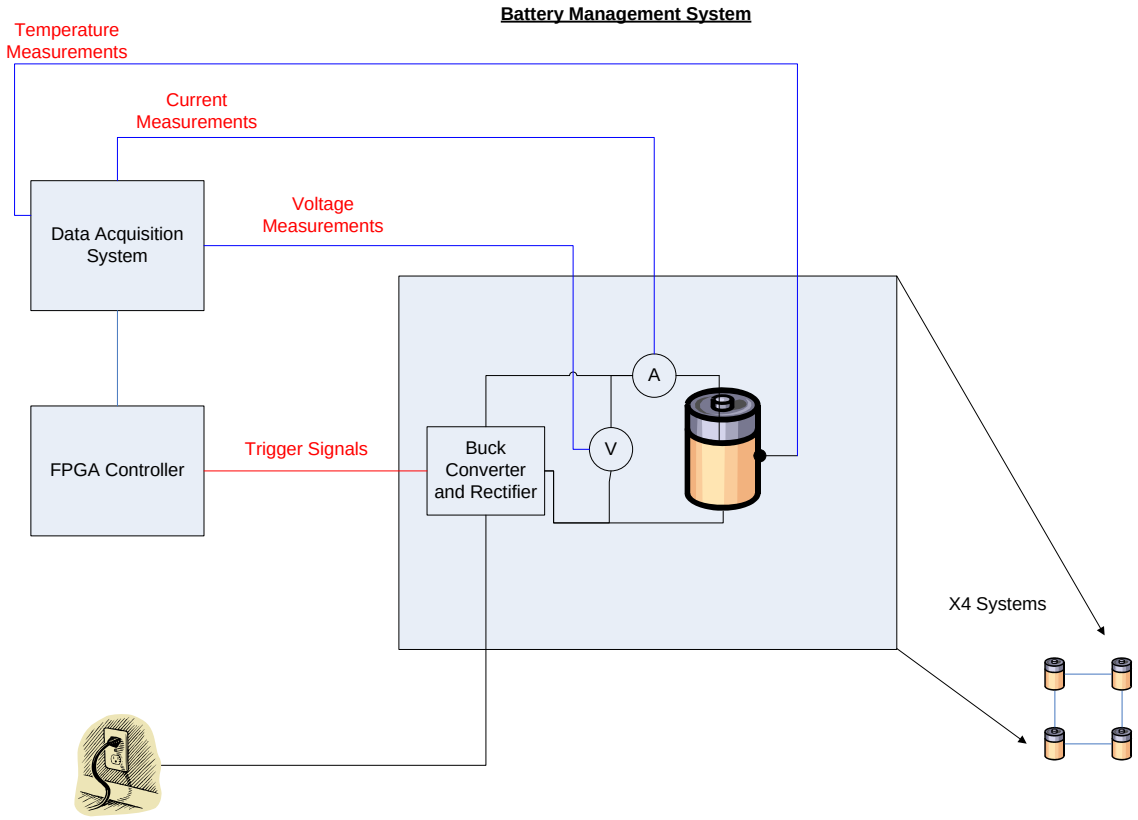

Figure 4. Functional Diagram of the Battery Management System. From [3].

The analysis documented in this thesis addresses the data acquisition from the buck converter and the conditioning of the voltage and current signals so they can be used to control battery charging.

The BMS uses three components to acquire and process the current for use in the FPGA. These components are the LEM sensor, the buffer/amplifier OPAMP, and the ADC. The relationship of these components is shown in Figure 5.

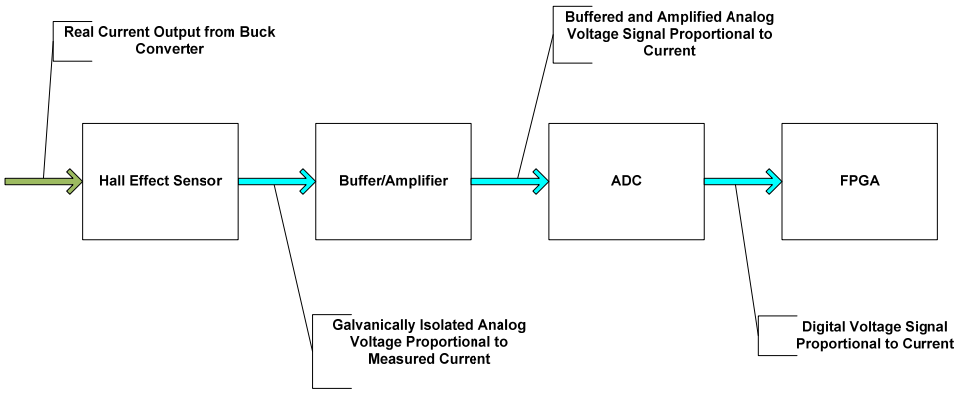

Figure 5. Current Signal Flowchart.

The voltage output of the buck converter has a much simpler path to the FPGA. The voltage to frequency converter measures and digitally converts the voltage signal to a digital square wave with frequency proportional to the measured voltage. The FPGA then converts this digital waveform to a scalar value. The control aspect of the FPGA uses this scalar value to control the operation of the BMS. The voltage processing is shown in Figure 6.

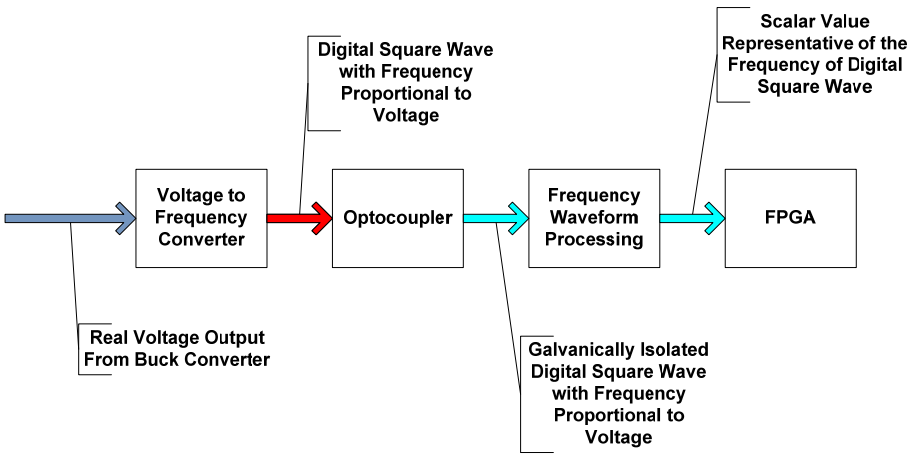

Figure 6. Voltage Signal Flowchart.

C. BUCK CONVERTER

The BMS uses a buck converter to deliver power to the Li-ion batteries for charging. The buck converter offers several advantages over other topologies including simplicity, ability to handle a wide range of voltages and currents, and high efficiency [3]. The buck converter used in the BMS uses a MOSFET switch operating at 30 kHz controlled by the FPGA. The FPGA varies the duty cycle D of the MOSFET switch to control the output current and the battery voltage. The charging current is constant until the battery voltage reaches an almost-full charge level. After the voltage reaches this level, the battery is trickle charged while regulating the voltage so as not to exceed the maximum battery voltage. The buck converter input-output voltage relationship is:

$$V_{out} = DV_{in}. \tag{1}$$

D. SENSORS POWER SUPPLY

The PCB interfacing with the FPGA includes a linear voltage regulator that outputs a constant 5 V. The power supply for the linear voltage regulator is the transformed and rectified DC signal from the transformer rectifier circuit. This voltage is 10 V. The PCB does not include a second linear voltage regulator to supply a −5 V. Therefore, all sensors on the PCB are single power supply sensors. This simplifies the design of the PCB, but slightly complicates the signal processing.

E. HALL EFFECT SENSOR

The Hall Effect Sensor used in the BMS is a current transducer made by LEM, model number HMS 20-P [5]. Its maximum current rating is 20 A, which is well above the expected current values during use of the BMS. The bandwidth of the sensor is 50 kHz, which is also well above the expected frequency of the current output of the buck converter. Like the other sensors, the Hall Effect Sensor uses a +5 V and ground as its power supply. As a result, the output voltage has an approximate 2.5 V offset from zero. The sensor's scaling and offset are:

$$V_{OUT} = V_{OE} \pm \frac{.625}{20} I_P . \tag{2}$$

and

$$V_{OE} = 2.5 \pm .025 \tag{3}$$

where I_P = Measured Current.

The voltage offset V_{OE} has a tolerance of .025 V. More precision than .025 V is required to accurately process the signal from the LEM sensor. Circuit testing will include procedures to empirically verify V_{OE}.

F. BUFFER AND INSTRUMENT AMPLIFIER

The LEM sensor is designed to output its signal to a device whose input impedance is greater than 200 kΩ [5]. The input impedance of the ADC is only 24 kΩ [6]. As is common in circuits, an amplifier buffers the LEM signal to provide this high impedance. The OPAMP used in the amplifier is a MCP619 Bi-CMOS OPAMP made by Microchip® [7]. The amplifier amplifies as well as buffers the LEM's signal. The amplifier is shown in Figure 7 and its DC gain A is [8]

$$A = 1 + \frac{6.8k}{10k} = 1.68 . \tag{4}$$

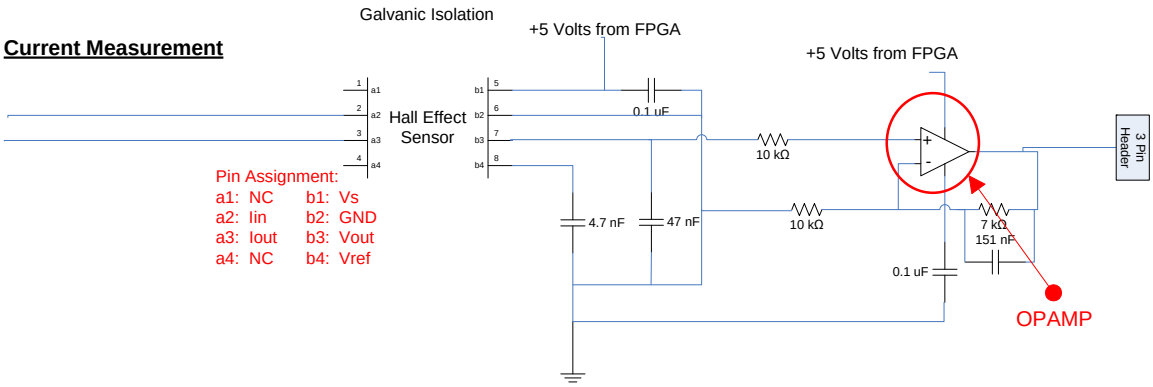

Figure 7. Instrumentation Amplifier. After [3].

The OPAMP circuit includes a capacitor that imparts high frequency stability. This design tool prevents high frequency signal noise from overdriving the OPAMP to saturation. The transfer function of the OPAMP, without the capacitor, would be

$$H(s) = 1 + \frac{R_f}{R_i} = 1 + \frac{6.8}{10} = 1.68. \tag{5}$$

The addition of the capacitor changes the transfer function to [8]

$$H(s) = 1 + \frac{R_f / R_i}{1 + sR_fC}. \tag{6}$$

At the frequency of the buck converter, Equation (6) becomes

$$\left|H(30{,}000 \cdot 2\pi \cdot i)\right| = \left|1 + \frac{.68}{1 + (2\pi \cdot i \cdot 30000Hz \cdot 10k\Omega \cdot 154nF)}\right| = 1. \tag{7}$$

The transfer function in Equation (6) does not amplify high frequency noise. As frequency rises, the second term goes to zero and gain becomes one. The frequency response of the OPAMP is shown in Figure 8.

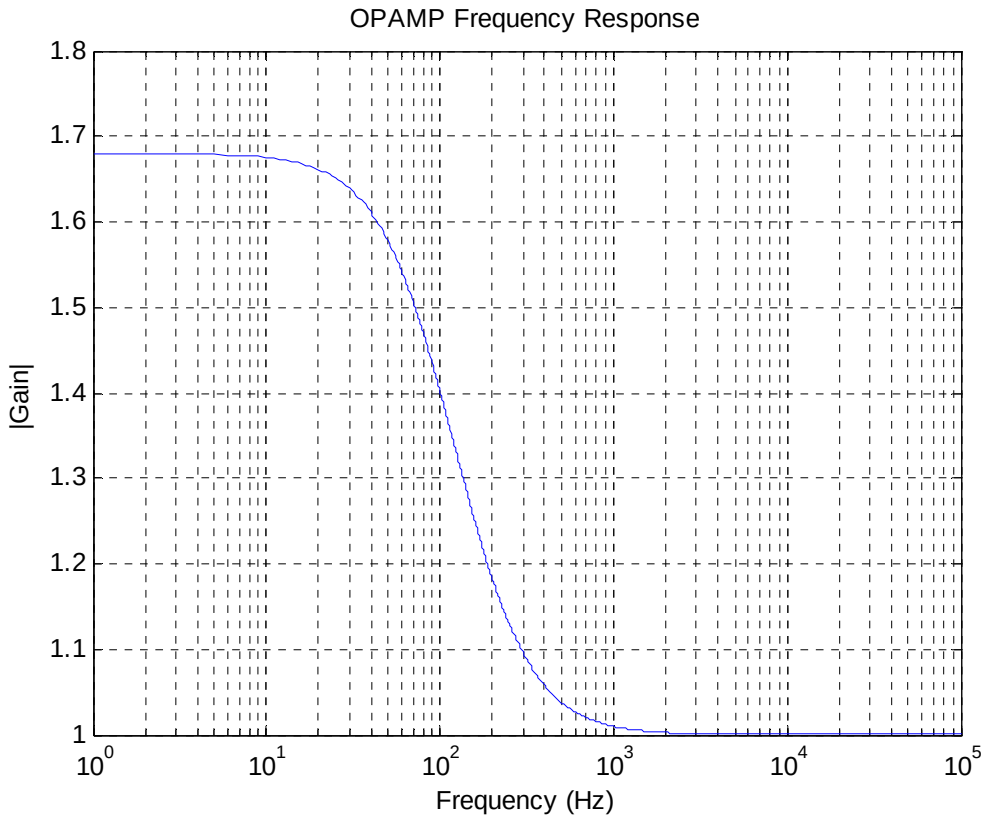

Figure 8. Amplifier's Frequency Response.

Theoretically, the frequency response of the amplifier goes to unity as frequency approaches infinity. The higher frequency signal content is passed to the A/D converter with unity gain. The capacitor on the output of the LEM sensor filters the higher frequency signal content.

To support this theoretical data, this thesis also documents a circuit simulation using PSpice Simulation Software. The simulated circuit is shown in Figure 9.

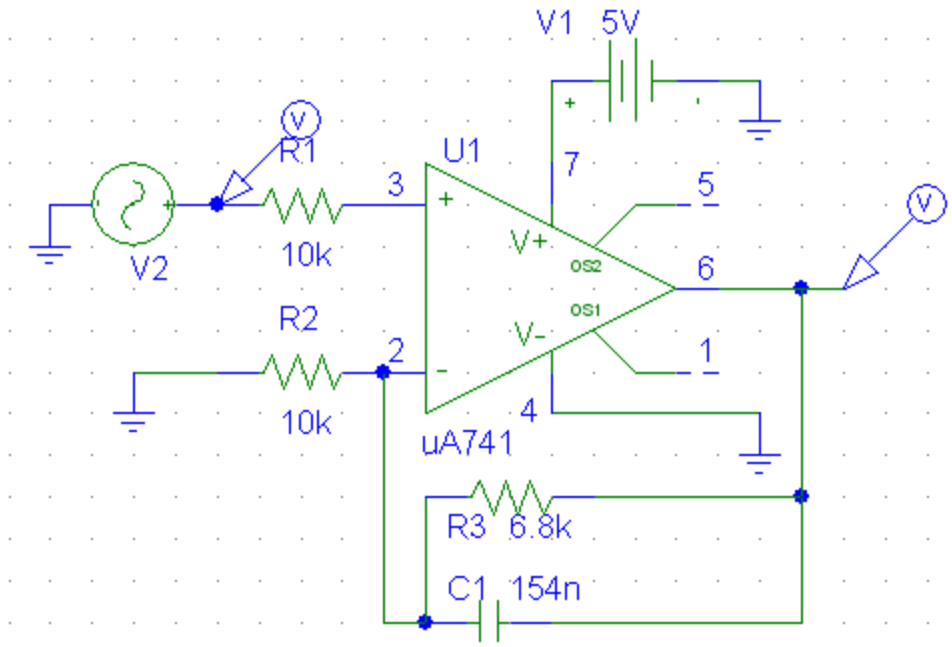

Figure 9. PSpice Amplifier Simulation Circuit.

The results of the PSpice simulation, shown in Figure 10, align well with theoretical calculations.

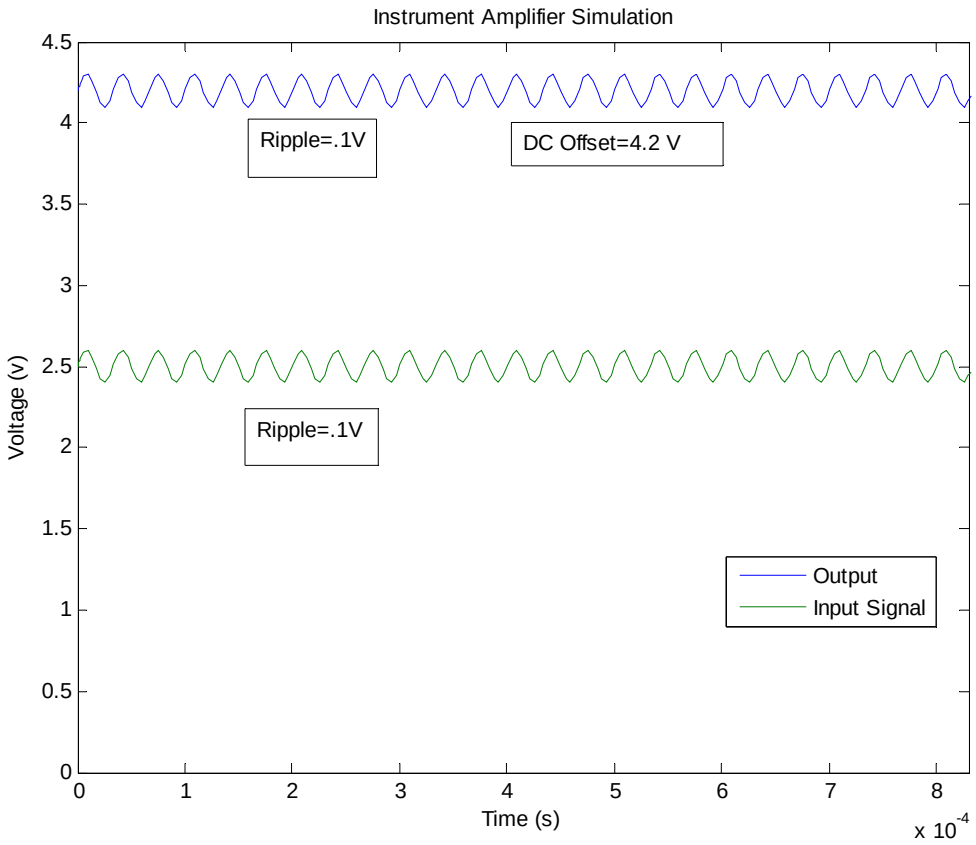

Figure 10. Instrument Amplifier Simulation Results.

For the simulation, the input signal is an AC voltage with frequency 30 kHz, 2.5 V DC offset, and 100 mV magnitude. This is similar to a typical voltage output from the LEM sensor. According to the simulation, the output from the amplifier would have a DC value of 4.2 V and the same magnitude of ripple. Thus, the AC gain is 1 and the DC gain A is

$$A = \frac{4.2}{2.5} = 1.68 . \tag{8}$$

This exactly matches the expected DC gain, as calculated in Equation (5).

At first glance, an alternative solution would be to use an inverting OPAMP in the instrument amplifier. Its transfer function would be

$$H(s) = \frac{-R_f / R_i}{1 + sR_f C} = \frac{-.68}{1 + s(.0015)} . \tag{9}$$

The frequency response of this amplifier is shown in Figure 11.

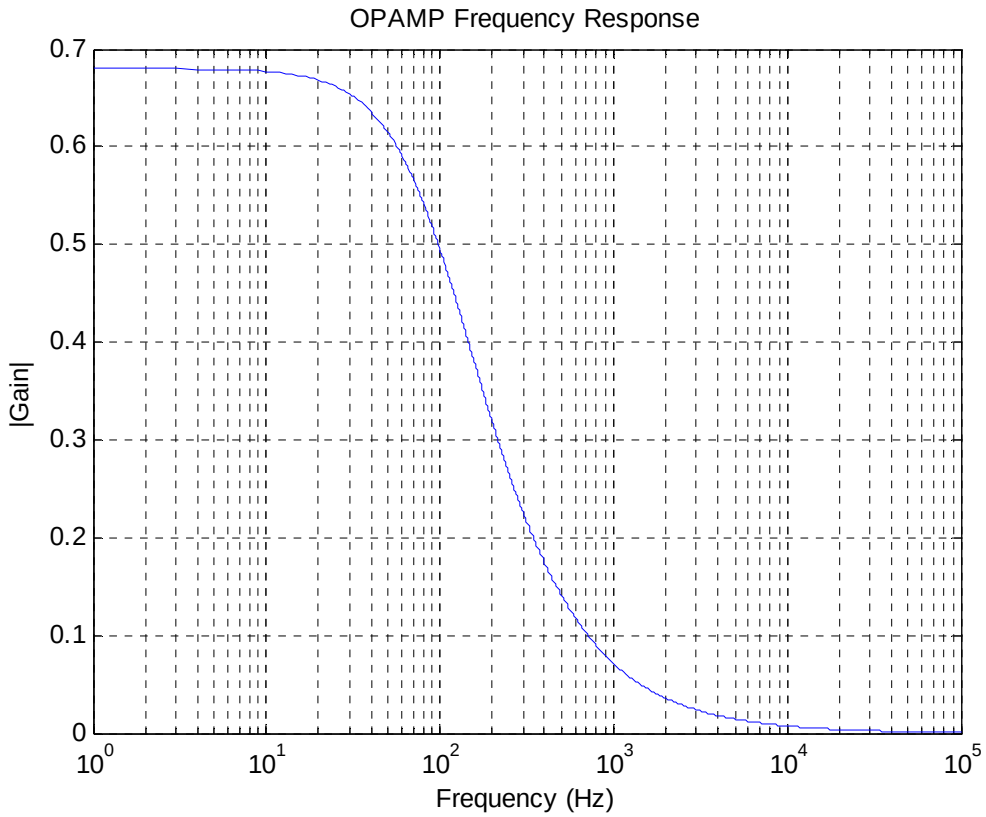

Figure 11. Inverting OPAMP Frequency Response.

This amplifier's gain is zero at 30 kHz and would completely filter the high frequency ripple in the signal. This solution is not possible since the unipolar power supply of the PCB prevents the use of an inverting OPAMP low pass filter. The inverting nature of the OPAMP requires a negative voltage power supply, which is not available for this application.

G. ANALOG TO DIGITAL CONVERTER

The ADC that samples both voltage and current is a 12-bit converter that also operates from a single 5 V power supply [7]. Its input impedance is 24 kΩ. It samples all signals in parallel so that the relative timing between samples of the signals is preserved. The sampling frequency of the ADC is 138 kHz. This rate is above the Nyquist sampling frequency [9], therefore, the ripple is fully transmitted to the FPGA for processing. The

proportional integrator controller compensates for this ripple by integrating this signal twice. The control gains are low which prevents the controller from responding to higher frequency signal content. This feature mitigates the impact of the ripple and noise in the current signal.

H. VOLTAGE TO FREQUENCY CONVERTER

A voltage to frequency converter measures the voltage output of the buck converter. The LM231, made by National Semiconductor, also requires a single voltage power supply for operation [10].

A simplified diagram of the LM231 is shown in Figure 12. At its core, the converter is a one shot timer triggered by a comparator. The input voltage V_{IN} is compared to a set voltage, V_X. If V_{IN} is greater than V_X, the comparator triggers the one shot timer with the pulse length:

$$T = 1.1 R_t C_t . \tag{10}$$

If V_{IN} is less than $V_{X,}$ the capacitor C_L discharges V_X until V_{IN} is greater than V_X and the comparator triggers the one shot timer.

The one shot timer sends a pulse to both the frequency output transistor and the switched current source. The pulse to the transistor creates the output frequency signal with period equal to the period defined by Equation (10).

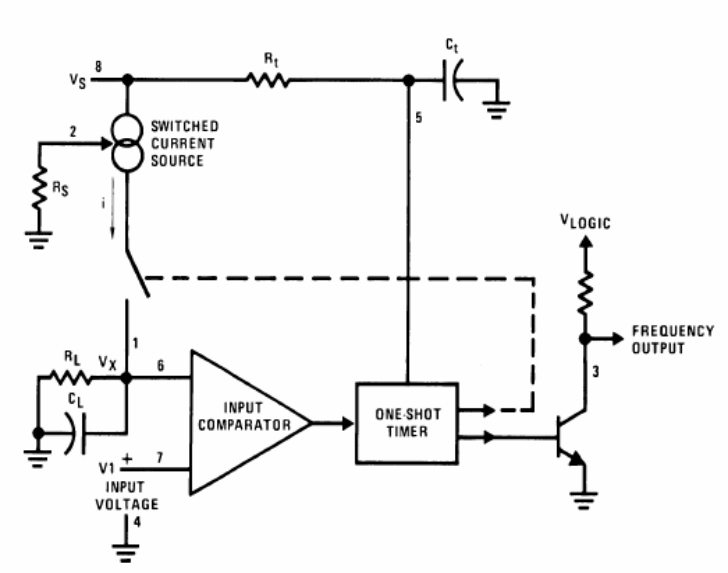

Figure 12. Simplified Circuit of V-to-F Converter. From [10].

The current source sends an exact amount of charge into the capacitor C_L.

$$Q = iT \tag{11}$$

This charge raises the voltage of V_X to a value higher than V_{IN}. Thus, at the end of the timing period, the comparator will not send a trigger signal and the one shot timer will reset. At this point, C_L discharges V_X until it falls below V_{IN} and the process begins again.

The current flowing into C_L is

$$I_{AVE} = i(1.1R_tC_t)\,f\ . \tag{12}$$

where f is the frequency of the one shot timer.

The current flowing out of C_L is

$$I_{OUT} = \frac{V_X}{R_L} \simeq \frac{V_{IN}}{R_L}\,. \tag{13}$$

If V_{IN} is doubled, the current out of C_L will also double and this causes the voltage at V_X to drop faster and shortens the time for the one-shot timer to reset, which lowers its frequency. The circuit reaches steady state once the frequency has also doubled to maintain the balance of charge at C_L.

The voltage-to-frequency converter's output is defined by

$$f_{out} = \frac{V_{in}}{2.09V}\frac{R_S}{R_L}\frac{1}{R_t C_t} = 1055.45 \cdot V_{in}. \quad (14)$$

The variables of Equation (14) are implemented in the BMS using the values contained in the following list:

- V_{IN} is the voltage measured by the voltage to frequency converter.
- R_S is the sum of the 12 kΩ resistor and 5 kΩ potentiometer (set at 3 kΩ)
- R_L is 100 kΩ
- R_t is 6.8 kΩ
- C_t is 0.01 uF

The square wave from the V-F converter drives an optocoupler so that the input signal to the FPGA is galvanically isolated from the battery charger.

I. FREQUENCY WAVEFORM PROCESSING

The FPGA receives a digital square wave signal with frequency proportional to the measured voltage. The frequency of this signal must be extracted from the waveform before the FPGA software can determine the voltage from the measured frequency. A SIMULINK® model created by Professor Alex Julian of the Naval Postgraduate School accomplishes this processing. The SIMULINK® model is shown in Figure 13.

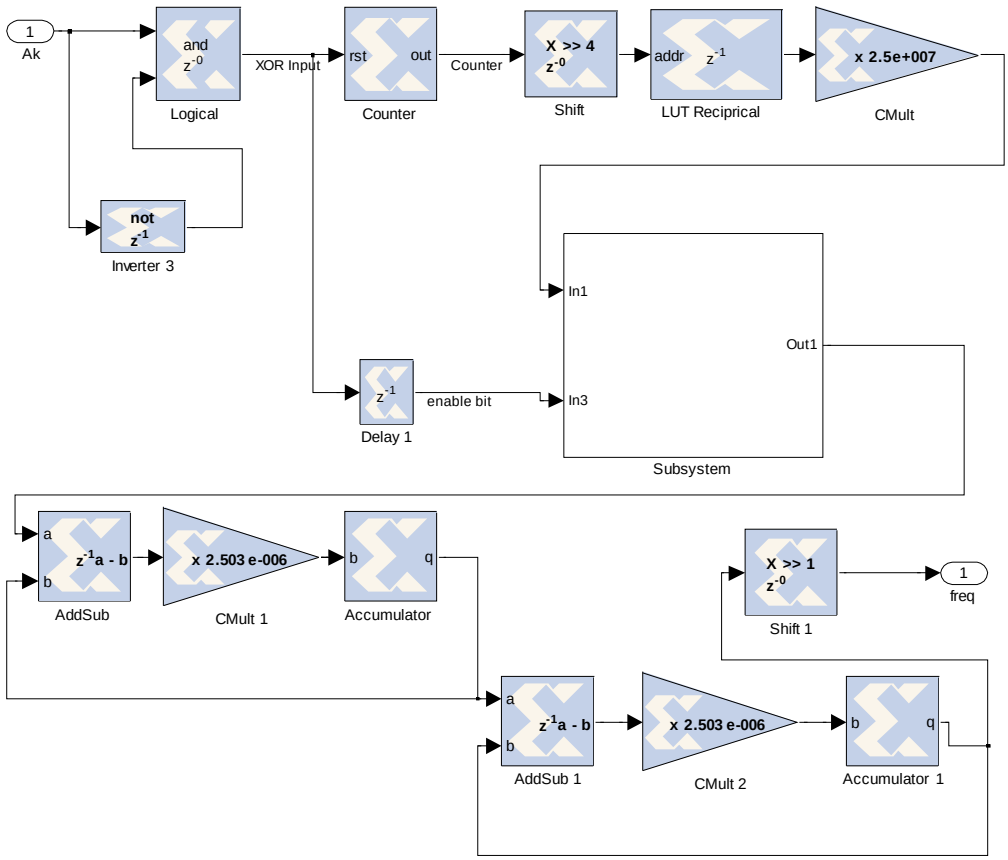

Figure 13. Frequency Waveform Processing Model.

The “and” and “not” blocks function as a rising edge detector to detect the leading edge of the square wave. The signal is now a pulse train with the same frequency as the original signal. The following counter counts the number of clock cycles at the frequency of the FPGA, 25 MHz. This is the number of periods of clock frequency between each pulse of the incoming signal. Essentially, it measures how much slower the incoming frequency is, relative to the clock frequency. The next three blocks: Shift, LUT Reciprocal, and “CMult,” accomplish division of the incoming values. The LUT Reciprocal is a look up table where the output y is

$$y = \frac{1}{x}. \tag{15}$$

This method implements the division function in a quick manner. As a tradeoff for the speed of calculation, the look up table occupies a large section of memory. To minimize this, the shift block reduces the 16 bit value to 12 bits to minimize the size of the look up table.

The "CMult" block adds a factor to the numerator, turning (15) into

$$y = \frac{2.5 \times 10^7}{x}. \tag{16}$$

where x is the number of clock cycles counted and 2.5 x 10^7 is the clock frequency of the FPGA. The result y is the frequency of the pulse waveform from the V-F converter.

The block marked, "Subsystem," in Figure 13, simply averages four consecutive values. As the voltage in the system changes slowly, this smoothing operation is appropriate. The final section is two low pass filters cascaded together to create a 2^{nd} order low pass filter. The result is a stable scalar that is the frequency of the received signal.

J. CHAPTER SUMMARY

The BMS consists of several components required for measuring and processing voltage and current signals relative to the battery. These components have theoretical effects on the signals that this chapter documented. These effects will be tested in the next chapter.

III. TESTING

A. INTRODUCTION

The BMS contains test points to enable monitoring of its behavior, but further test points are necessary to thoroughly test the system. The feedback control of the buck converter is disabled during sensor testing in this chapter.

B. TESTING CIRCUIT

The circuit has several test points to allow for analysis throughout the circuit. These points are listed in Table 1.

Table 1. Test Points.

Test Point #	Signal Measured
1	Voltage into the MOSFET Switch
2	Voltage Provided by the Linear Regulator
3	Ground of the Buck Converter (At Linear Regulator)
4	Output of the Current Sensor before Amplification
5	Ground of the Buck Converter (At the bleed resistor)
6	Switching Signal into the MOSFET Driver
7	Voltage out the Voltage to Frequency Converter
8	Voltage after the MOSFET Switch
9	MOSFET Driver Bootstrap Voltage

The work documented in this thesis extensively used certain test points for analysis. The circuit, with the applicable test points used for this thesis, is shown in Figure 14.

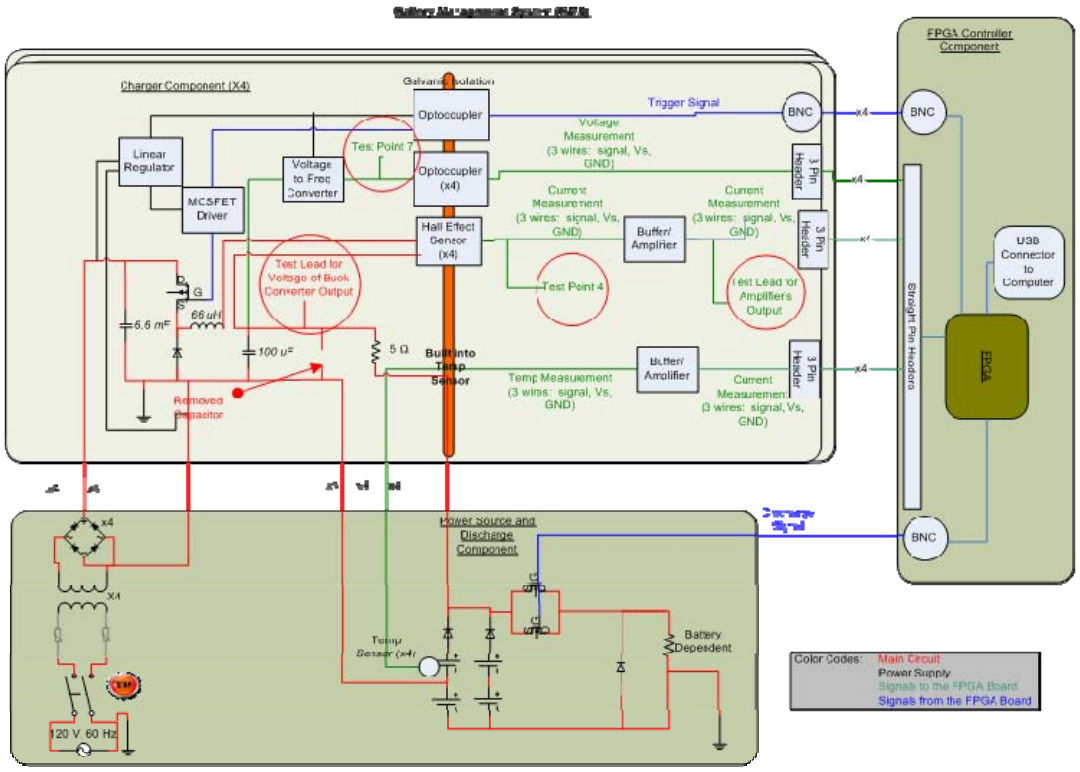

Figure 14. BMS. After [3].

The first step in testing was to recreate the signals generated during normal operation. This could be done using the circuit as is, and using the FPGA to control the trigger to the buck converter and therefore the output of the BMS. This method would have been somewhat complicated and become onerous to continuously modify for testing. Instead, an Agilent 33220A 20 MHz function generator replaced the FPGA as the source of the trigger signal. This allowed for easy manipulation of both the frequency and duty cycle of this signal. For testing, the waveform transmitted to the MOSFET was a 3 V peak-to-peak square wave with a 1.5 V DC offset.

The second modification made for signal recreation was to disconnect the transformer rectifier as the power source for the buck converter and associated sensors. A GW Instek, GPC 3030D, Laboratory Power Supply would instead supply the necessary power. The power supply operated at 10 V DC and supplied the current pulled by the buck converter, the load resistor and sensors.

Analysis of the voltage signal required no further modifications to the circuit in Figure 14. Test point 7 contains the output of the V-to-F converter. The current signal analysis did require circuit modification to measure the true current output of the buck converter. As designed, the buck converter's output is filtered by a 100 uH capacitor and is dissipated by a 2 kΩ resistor. Removing these components was necessary to measure the actual current output of the buck converter.

After removing the capacitor and resistor, the current loop was extended to an external 100 W, 5 Ω resistor. A Tektronix A6303 Current Probe measured the current passing through the external resistor and a Tektronix TM502A Current Probe Amplifier transmitted this measurement to a Tektronix TDS 3012B Oscilloscope for analysis. The probe's signal was very clean and easy to read so it served as the trigger source for all future current analysis on the oscilloscope.

C. TESTING PROCEDURE

1. Current Signal

In order to recreate the signal generated by the buck converter during normal operation, the waveform generator transmitted a 30 kHz trigger signal at duty cycles of 20%, 80%, and 50%. These duty cycles create waveforms that are clearly DCM, clearly CCM, and shortly after the onset of CCM, respectively.

The signal from the current probe is compared to the output from the LEM Hall Effect Sensor, the Low Pass Filter OPAMP, and the Analog to Digital Converter for analysis. Test point four provides the signal from the LEM Hall Effect Sensor. The output of the OPAMP does not have a test point, but it is possible to clamp onto the 151 nF feedback capacitor to sample output voltage. The original SIMULINK® model included an output to Chipscope for the current, voltage, and temperature signal. This allowed the signal from the ADC to be viewed on the Chipscope plotter window for analysis and comparison. The MATLAB® code necessary to decode and plot the Chipscope data is given in Appendix A.

The Tektronix Oscilloscope received each of these signals, except the ADC output, for analysis. This model oscilloscope has an Ethernet adapter that allows an internet browser to view the output of the oscilloscope. Further, MATLAB® can import the actual data plotted on the oscilloscope for analysis. Importing this data is as simple as placing the exported file in the working MATLAB® directory, right clicking on it, and selecting, “Import data.” The first four elements of the signal array are header information. After import into MATLAB®, analysis of the array required deleting these elements from the array.

Due to the small ripple of the LEM sensor output and the 2.5 V DC offset, DC coupling on the oscilloscope was not possible. The ripple required more zoom than could be offset with the oscilloscope so it was not possible to view the signal when appropriately zoomed in and in DC coupling mode. To solve this issue, the oscilloscope was set to AC coupling (for the sensor signals) and a multimeter that was in parallel to the oscilloscope measured the DC component of the signal. This value is the DC offset lost by AC coupling on the oscilloscope.

Testing also included data at 8 kHz to see what effect a slower converter frequency would have on performance.

To summarize, this procedure created and sampled eighteen current signals. Nine signals each of 30 kHz and 8 kHz. Once collected, sampled, and exported into MATLAB®, the twelve signals from the LEM sensor and OPAMP required the appropriate scaling and offset to allow comparison to the current probe signal.

For each of these signals, the first step was to apply the offset that the multimeter recorded. Next is to apply the appropriate scaling. Restoring this signal to Amps requires subtracting the offset of 2.49 V and then multiplying by 32, which is the inverse of the scaling factor in Equation (2).

The output of the OPAMP required the same procedure as the LEM sensor signal, but a scaling factor added to the offset. The OPAMP’s DC gain is 1.68 and 30 kHz gain is 1. The extraction procedure is

$$I = \frac{(V_{out} - (2.49 \cdot 1.68))}{1 \cdot 32}. \quad (17)$$

2. Voltage Signal

The signal from the voltage to frequency converter is a digital signal of varying frequency. This negates the need for an ADC to process the signal before reaching the FPGA.

During operation of the BMS, the voltage output of the buck converter typically ranges from 3 to 4 V. Since the load used for testing is significantly different from the Li-Ion batteries that are normally the load, this voltage range does not correlate to the duty cycles used during the current signal testing.

Due to the simplified flow path of the voltage signal, adequate testing was possible with significantly fewer measurements. The required measurements were the DC value of the output voltage, the frequency waveform from the voltage to frequency converter, and the frequency value that the FPGA software determines from the frequency waveform.

The testing circuit is a slightly modified version of the testing circuit of the current signal. A multimeter measured the DC value of the output voltage from the buck converter. The oscilloscope sampled the output of the voltage to frequency converter. These two measurements enabled the comparison of input voltage to output frequency of the voltage to frequency converter.

The last element of the voltage signal is the conversion from a digital frequency waveform to a single scalar value that represents the frequency. The FPGA circuit accomplishes this conversion. Chipscope sampled the resultant value for later in analysis.

D. CHAPTER SUMMARY

Recreating the current signal in a controlled, measureable fashion required modifications to the PCB as well as various supporting equipment. Due to the easier

nature of voltage measurements and the few components in the voltage signal flow path, voltage testing required less preparation. The results of both voltage and current testing are contained in Chapter IV.

IV. MEASUREMENT RESULTS

A. INTRODUCTION

The testing in Chapter III provides thorough analysis and documentation of voltage and current signal processing. This chapter presents the results of this testing.

B. CURRENT SIGNAL

1. Signal Processing

The waveforms from each sensor required separate processing specific to that sensor. The LEM sensor has the output shown in Equations (2) and (3). In addition the output voltage, there is another variable in these equations: V_{OE}. This voltage is $2.5 \pm .025$ V [4]. This error of .025 V becomes .8 V when multiplied by the scaling factor 32. This error is not defined well enough to allow for adequate analysis. An additional experiment is necessary to accurately define V_{OE}. Manipulating (2) and (3), we get

$$V_{OE} = V_{OUT} - \frac{I_{IN}}{32}. \tag{18}$$

This experiment sent a constant current to the LEM sensor by keeping the MOSFET switch in the buck converter constantly open. An external probe measured the output current of the converter to provide the true current into the LEM sensor. The results of this experiment are shown in Table 2.

Table 2. Offset Voltage Experiment Data.

Current In (Amps)	**LEM Output Voltage**	**Calculated V_{OE}**
0.64	2.505	2.485
0.77	2.509	2.485
1.02	2.517	2.485
1.2	2.523	2.485

The results show that the LEM sensor's V_{OE} is constant over the range of input current. The value 2.49 V is used for all current signal processing. The same data allows for accurate calculation of the LEM sensor's gain. The average scale factor of the four sets of data matches the datasheet's value of 32.

The output waveforms of the sensor and OPAMP contain high frequency noise in the signal. A low pass filter removes this noise to enable complete analysis. The MATLAB® function in Appendix B is this filter by creating the Fourier series coefficients of an input signal. It then recreates the signal in the time domain using the first X number of Fourier series coefficients, where X is an input to the function. This filters out the high frequency components of the signal, thereby removing the high frequency noise present. For the work presented here, the MATLAB® code recreated the signal using the first 200 Fourier Series Coefficients. This filters the signal to a sharp bandwidth limit of 100 MHz. This function filtered all current signals to allow for clear comparison. The effects of the low pass filter code on a signal collected from the BMS are shown in Figure 15.

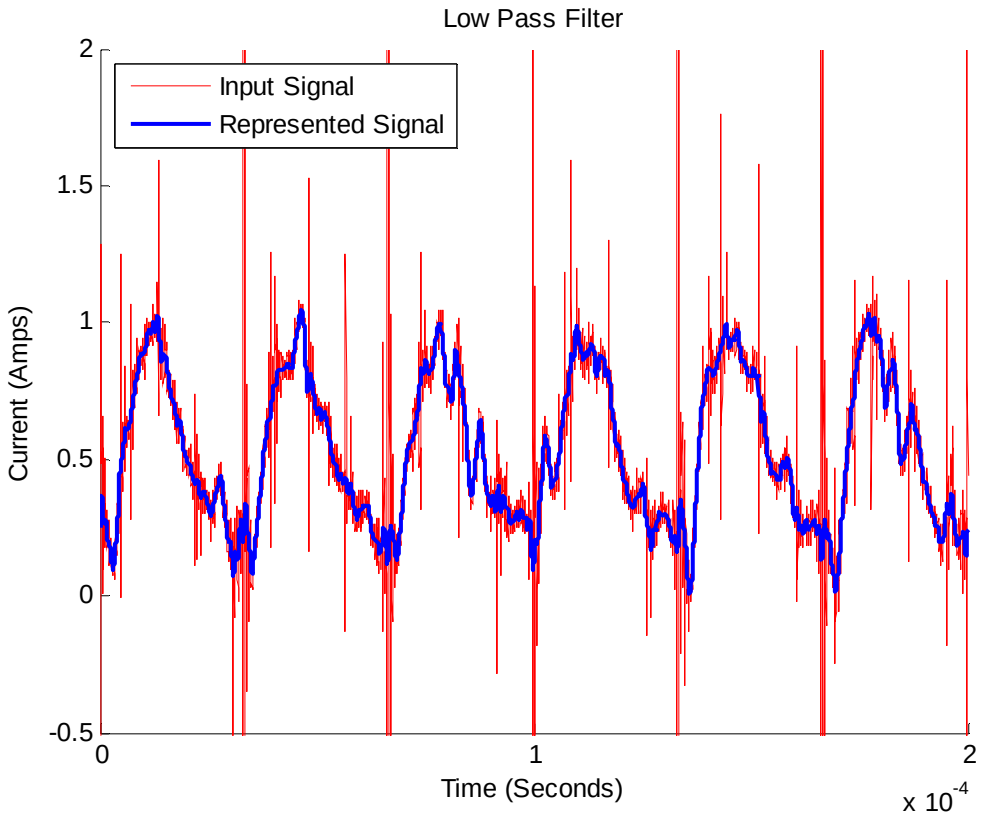

Figure 15. Low Pass Filter of Output from LEM Sensor.

The filter cleanly filters out the noise present in the signal while adequately preserving the input waveform.

2. 30 kHz Data

The BMS operates at 30 kHz so analysis will begin with this data. The processed, but unfiltered, data demonstrates accurate signal measurement by the LEM sensor and signal reproduction by the OPAMP. The signals are shown in Figure 16. There is minimal distortion of each signal. The probe is clearly the cleanest signal with zero noise. The LEM sensor has more noise and variations to the waveform. The OPAMP has a similar amount of high frequency and low frequency noise.

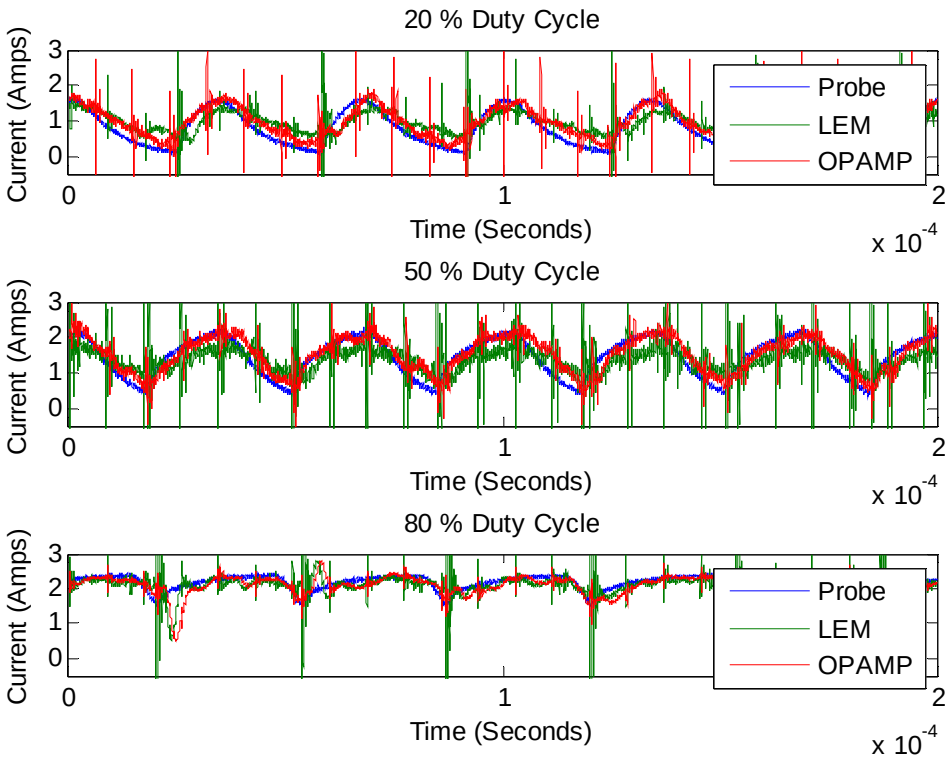

Figure 16. 30 kHz Current Signal (Unfiltered).

Filtering the signals with the code in Appendix B allows for a more precise analysis of the waveforms. As shown in Figure 17, the LEM sensor accurately replicates the general shape of the current waveform of the probe signal. The sensor does introduce random events into the waveform that causes deviation from the original waveform. Interestingly, the OPAMP replicates these events to various degrees. At 20% duty cycle, the OPAMP signal is very smooth and contains almost no random noise in its signal. At 50% duty cycle, the OPAMP's output remains smooth, while containing slightly more noise from the LEM Sensor. At 80%, the OPAMP replicates almost all noise that the LEM sensor transmits. When at 80% duty cycle, the converter is well into CCM and has very little ripple. As a result, the voltage input to the OPAMP is changing more slowly. This allows the OPAMP to respond to the small, higher frequency, change in voltage.

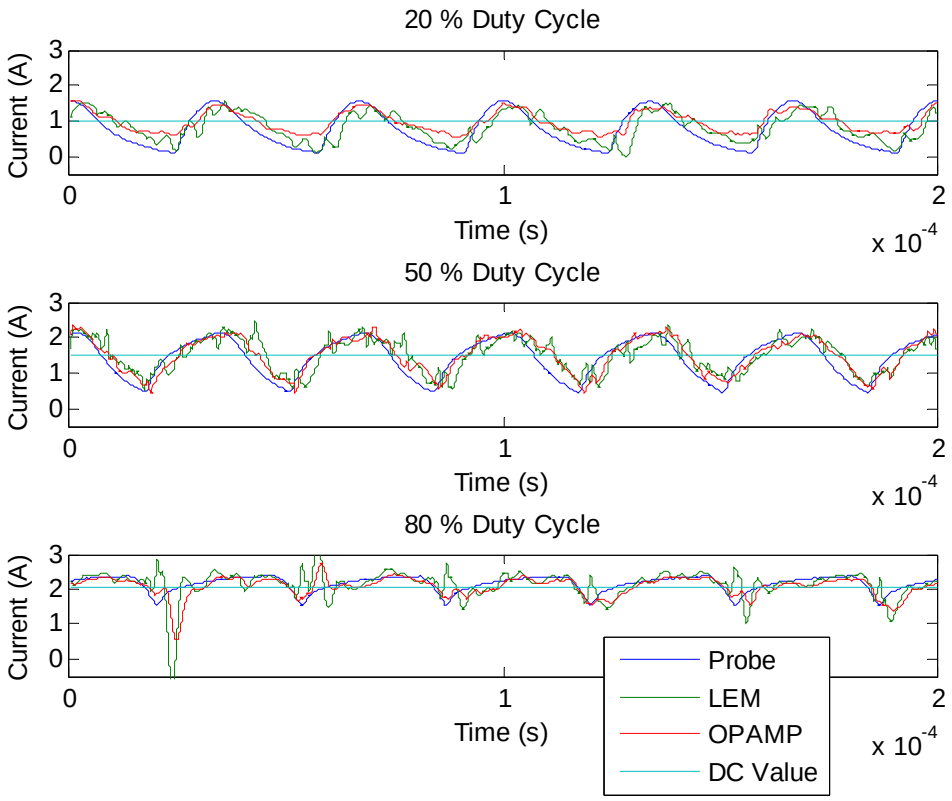

Figure 17. 30 kHz Current Signal (Filtered).

As shown in Figure 5, the output from the OPAMP is converted to a digital signal for use by the FPGA. The BMS SIMULINK® model includes a means for viewing this signal in Chipscope. These signals, for each duty cycle, are shown in Figure 18.

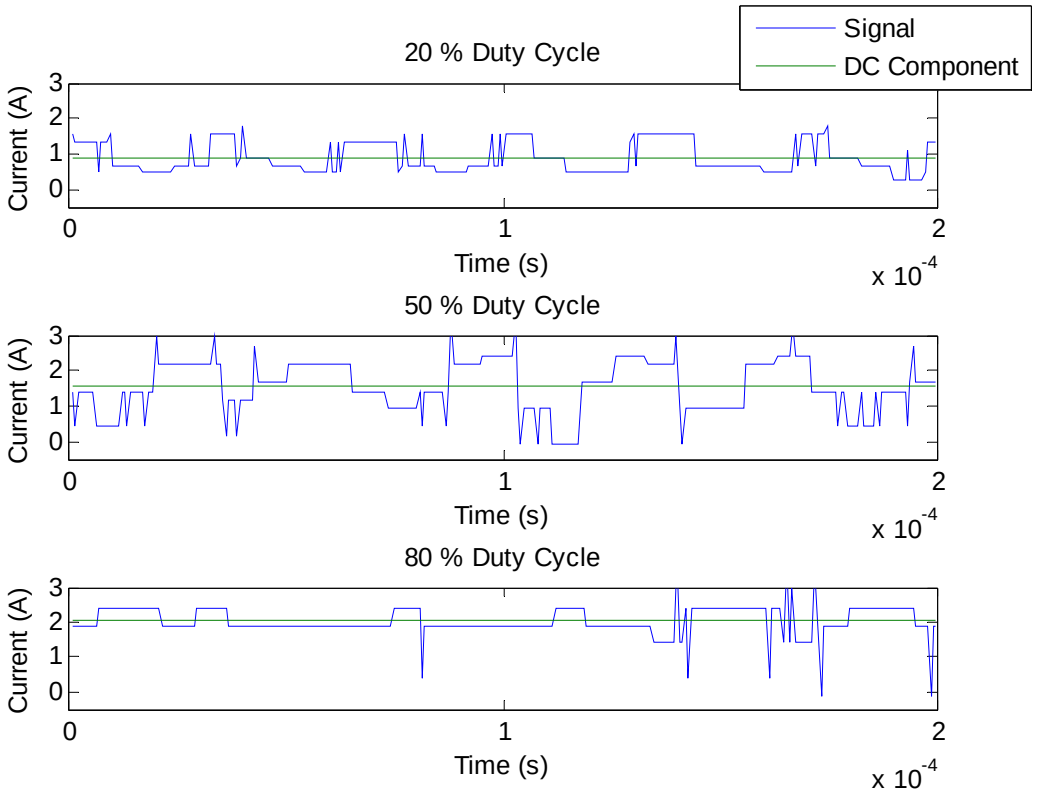

Figure 18. 30 kHz Digital Signals.

Comparisons between Figure 18 and Figure 17 show that the digital signals show significant deviation from the input to the ADC. There is significant quantization error and there are random noise spikes in the data. This error does mainly apply to the waveform's shape, not the waveform's DC component value. Comparison between Figure 17 and Figure 18 shows that the DC component for each duty cycle is successfully transmitted to the FPGA. Since the charger controller responds slowly to changes, the average value of the measured current most strongly affects the controller behavior.

3. 8 kHz Data

The signals measured from the BMS when operating at 8 kHz are much cleaner than those at 30 kHz. The filtered current signal from the current probe, LEM sensor, and OPAMP are shown in Figure 20 while the unfiltered data is shown in Figure 16. The LEM sensor has noticeable noise caused deviation from the current probe signal. In a

similar fashion as the 30 kHz case, the OPAMP filters out when the signal is quickly changing value. This filtering is significantly diminished when the current value is relatively constant.

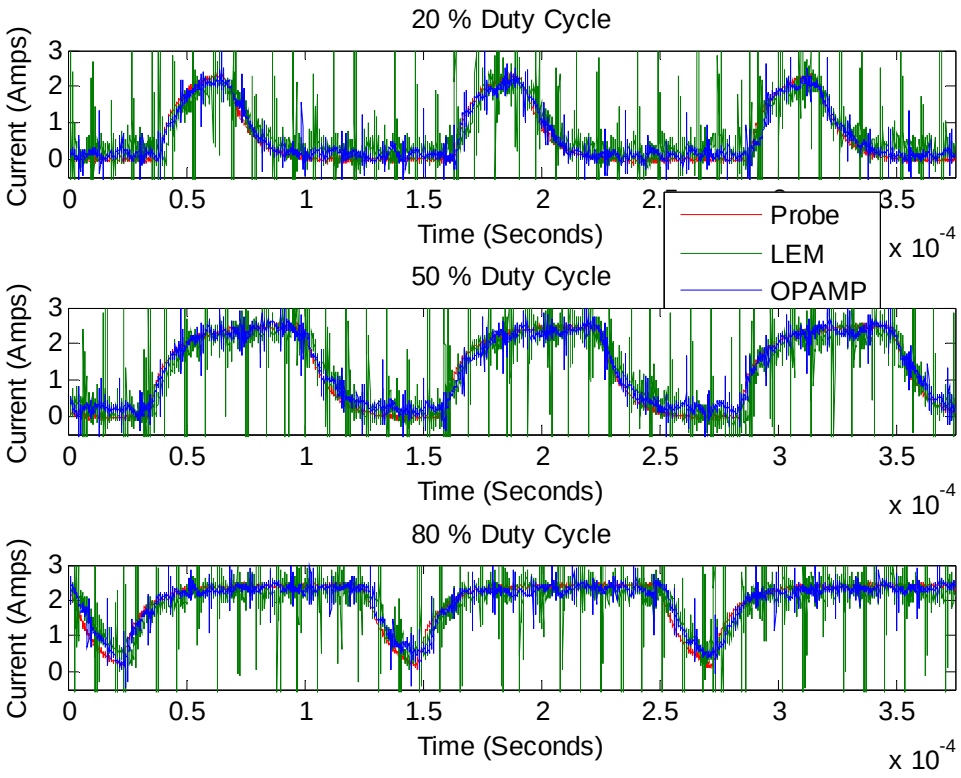

Figure 19. 8 kHz Current Signal (Unfiltered).

As in the 30 kHz case, the DC component of Figure 20 is the DC component input to the ADC.

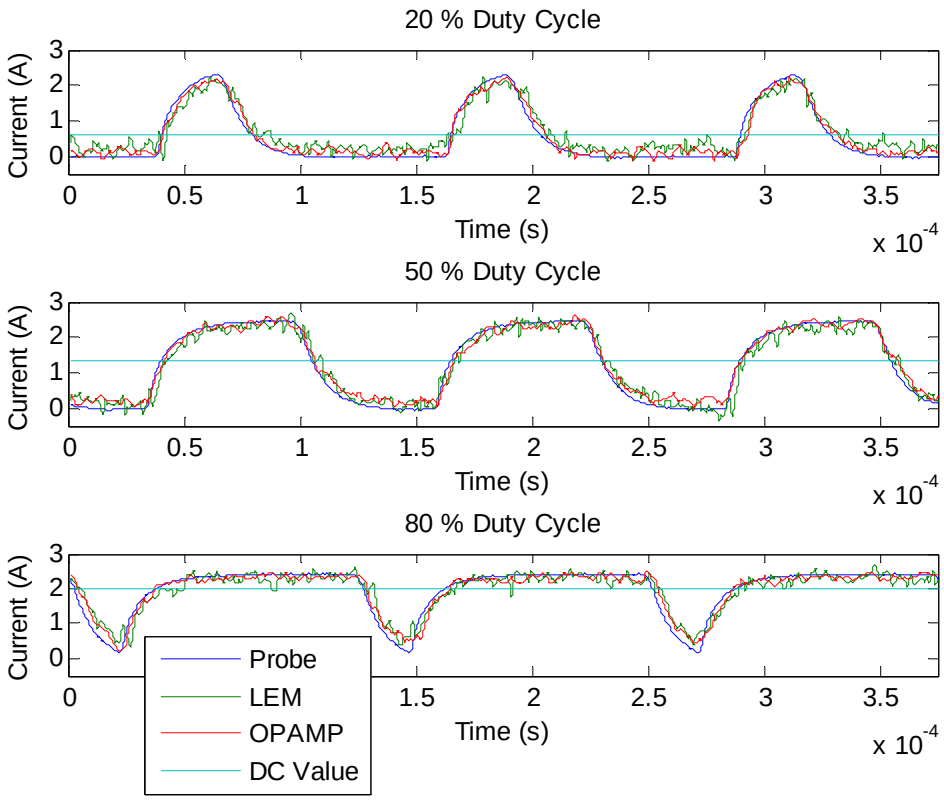

Figure 20. 8 kHz Current Signal (Filtered).

Also similar to the 30 kHz case, the ADC introduces significant distortion to the waveform, but the DC component remains consistent with the input to the ADC.

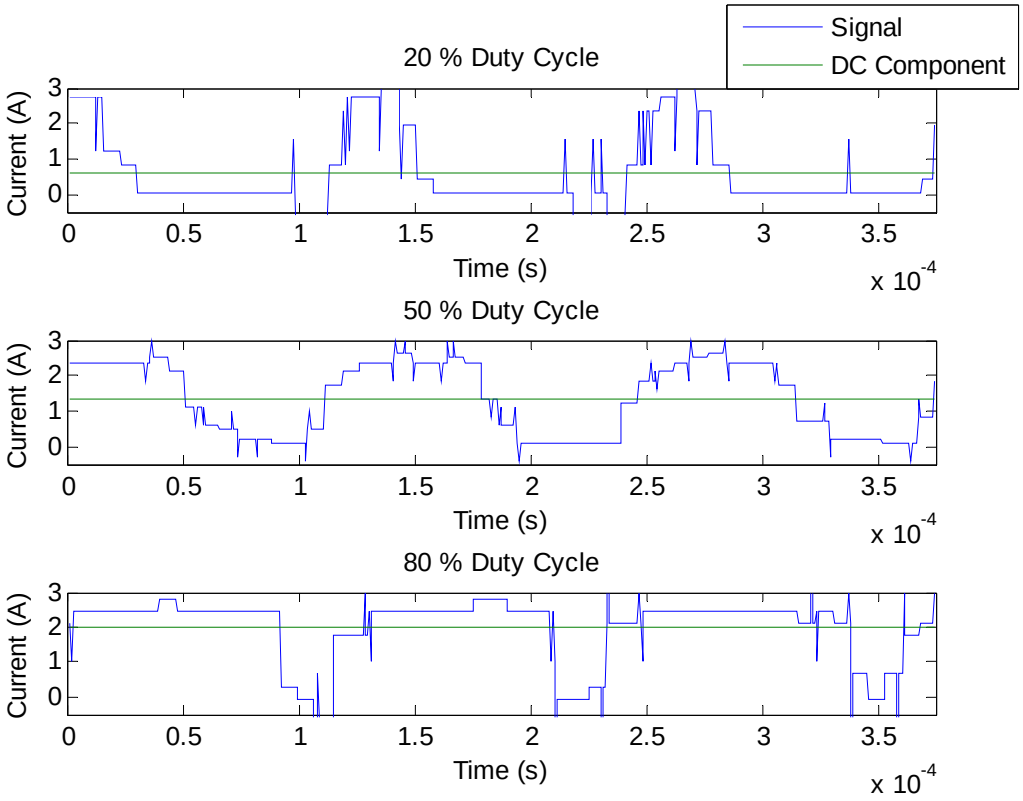

Figure 21. 8 kHz Chipscope.

C. VOLTAGE SIGNAL

The voltage signal's flow path is much simpler than the current signal. The Voltage to Frequency converter's output is a digital square wave so there is no need for an ADC. The FPGA simply records the output from V-to-F converter for processing. The frequency waveform from a measured 3.5 V is shown in Figure 22.

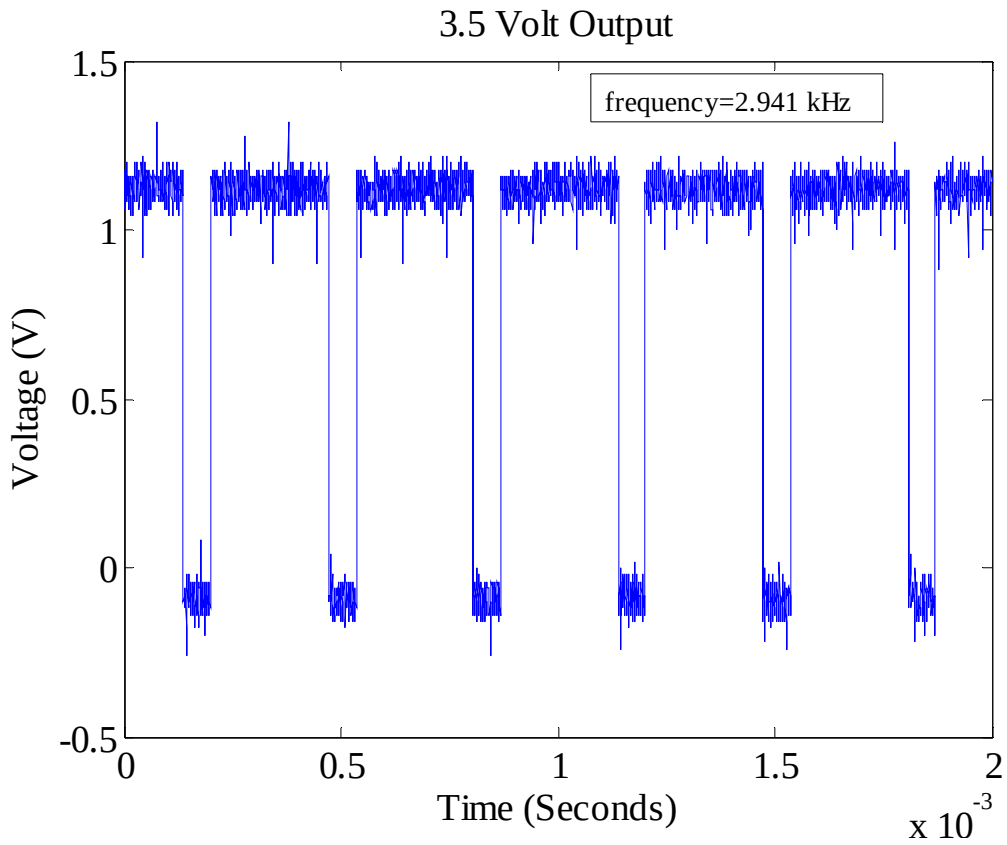

Figure 22. 3.5 Volt Output from V-to-F Converter. Output Frequency = 2.941 kHz.

As with the current signal, the voltage signal passes through a Chipscope interface. Due to the FPGA's 2nd order low pass filter and data averaging; the output is a straight line at 3,042 Hz. This is a 3% error in frequency. After scaling according to Equation (19), this error corresponds to less than 1% error in measured voltage.

The frequency of the waveform in Figure 22 should match the theoretical frequency predicted by Equation (14). This is not the case. Rearranging (14) and substituting the data from Figure 22 to find the true scaling factor *S* yields

$$S = \frac{2941}{3.5} = 840.37 \text{ Hz/V}. \tag{19}$$

This is significantly different from the theoretical scale value of 1,055.54. This fact does not impede the operation of the BMS as the processing accounts for this discrepancy by using an empirically determined scale factor. The data used to determine this scale factor is shown in Table 3.

Table 3. V-to-F Converter Calibration Data.

Voltage (V)	**2.73**	**2.97**	**3.13**	**3.21**	**3.4**	**3.65**	**3.85**	**4.04**
Frequency (kHz)	2.35	2.52	2.65	2.75	2.86	3.1	3.35	3.44

Plotting this data in MATLAB® and then using the built in data-fitting tool allows a simple method to extract a linear equation to fit this data. The data fitting is shown in Figure 23.

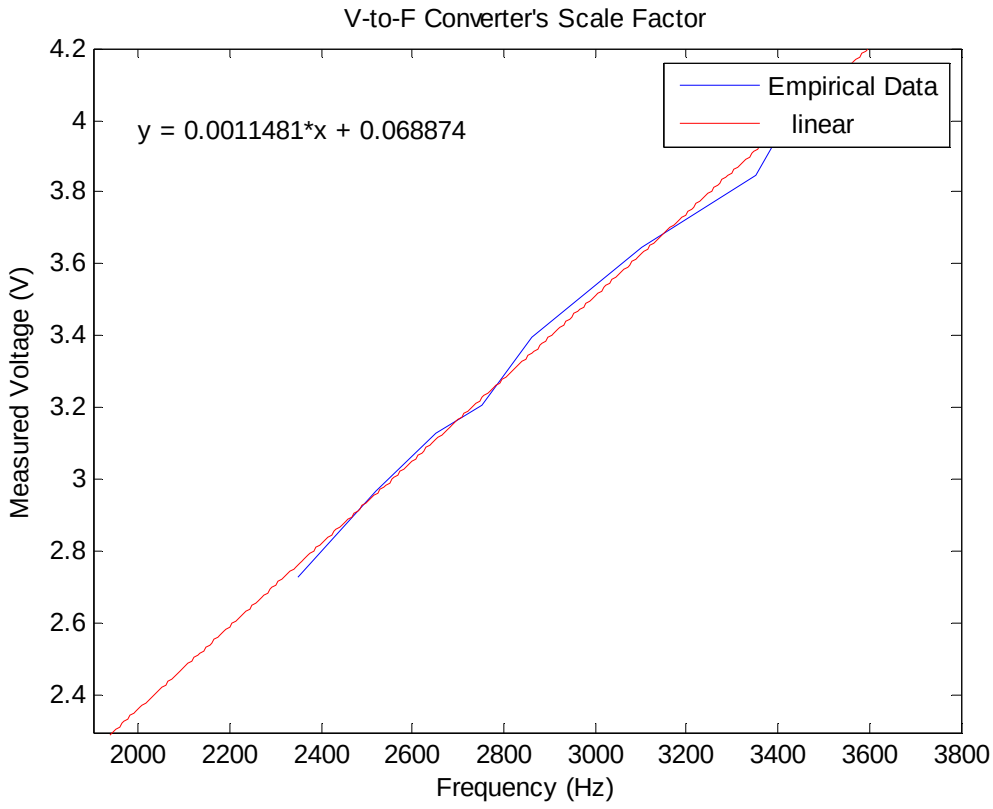

Figure 23. Linear Equation to Fit Data.

The slope of the fitted equation is the inverse of the scale factor of Equations (14) and (19). The inverse of the equation's slope is 871. This scaling factor is used for frequency waveform processing for this applicable card.

As with the current signal, the voltage signal passes through a Chipscope interface. Due to the FPGA's 2nd order low pass filter and data averaging, the output is a straight line at 3,042 Hz.

D. CHAPTER SUMMARY

The results of the testing described in Chapter III were presented in this chapter. Testing showed the BMS to properly measure and process the voltage and current produced by the buck converter. Context to the results of this chapter, and possible future work to improve the BMS, are given in Chapter V.

V. CONCLUSION

A. SUMMARY

The Naval Postgraduate School's BMS serves as research platform to push forward a required technology to advance the Navy's plan for highly automated, integrated electric drive ships.

The aim of this thesis was to improve BMS's performance by conducting thorough testing during simulation of actual use. Testing at both 30 kHz and 8 kHz and at three different duty cycles, at each frequency, allowed for a clear comparison of performance at various real and theoretical operating conditions.

The testing results showed that, when properly calibrated, the BMS properly measures and transmits voltage data to the FPGA for processing and control. The current signal undergoes significant waveform distortion during the digital conversion. The DC component remains intact. The buck converter's PI controller properly deals with this distortion by slowly responding to rapid changes in current. This allows the controller to respond only to the correct DC component of the current signal.

B. FUTURE WORK

There are several areas where research could improve the operation of the BMS:

- Expand the FPGA's programming to manage all four batteries.
- Calibrate the two remaining PCBs.
- Develop programming to automatically calibrate each PCB.
- Develop a hardware solution to support calibration programming.
- Determine optimal charging strategies.
- Explore the use of non-inverting OPAMPS as low pass filters.
    - Specifically, analyze the use of an RC low pass filter in series with the amplifier.
- Create software to test and manage various other batteries.

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APPENDIX A. CHIPSCOPE DATA PLOT CODE

Courtesy of Professor Alex Julian of the Naval Postgraduate School

```
datain=importdata('3V.prn');
vecsize=length(datain.data);
deltat=1/(25e6/2^4);
% datasize=round(1/60/deltat);
datasize=vecsize-1;
adc1raw=zeros(1,datasize);
adc2raw=zeros(1,datasize);
adc3raw=zeros(1,datasize);
adc4raw=zeros(1,datasize);
for ii=1:datasize
   index=ii+vecsize-datasize-1;

adc1raw(ii)=datain.data(index,1+2)+2*datain.data(index,2+2)+2^2*datain.data(index,3+
2)+...
      2^3*datain.data(index,4+2)+2^4*datain.data(index,5+2)+...
      2^5*datain.data(index,6+2)+2^6*datain.data(index,7+2)+...
      2^7*datain.data(index,8+2)+2^8*datain.data(index,9+2)+...

2^9*datain.data(index,10+2)+2^10*datain.data(index,11+2)+2^11*datain.data(index,12+
2);


adc2raw(ii)=datain.data(index,1+14)+2*datain.data(index,2+14)+2^2*datain.data(index,
3+14)+...
      2^3*datain.data(index,4+14)+2^4*datain.data(index,5+14)+...
      2^5*datain.data(index,6+14)+2^6*datain.data(index,7+14)+...
      2^7*datain.data(index,8+14)+2^8*datain.data(index,9+14)+...

2^9*datain.data(index,10+14)+2^10*datain.data(index,11+14)+2^11*datain.data(index,1
2+14);


adc3raw(ii)=datain.data(index,1+26)+2*datain.data(index,2+26)+2^2*datain.data(index,
3+26)+...
      2^3*datain.data(index,4+26)+2^4*datain.data(index,5+26)+...
      2^5*datain.data(index,6+26)+2^6*datain.data(index,7+26)+...
      2^7*datain.data(index,8+26)+2^8*datain.data(index,9+26)+...
```

```
2^9*datain.data(index,10+26)+2^10*datain.data(index,11+26)+2^11*datain.data(index,1
2+26);


adc4raw(ii)=datain.data(index,1+38)+2*datain.data(index,2+38)+2^2*datain.data(index,
3+38)+...
      2^3*datain.data(index,4+38)+2^4*datain.data(index,5+38)+...
      2^5*datain.data(index,6+38)+2^6*datain.data(index,7+38)+...
      2^7*datain.data(index,8+38)+2^8*datain.data(index,9+38)+...

2^9*datain.data(index,10+38)+2^10*datain.data(index,11+38)+2^11*datain.data(index,1
2+38);

end

adc1=((((adc1raw/2^6)-1))/1.736-2.5)*20/.625;
adc2=adc2raw/2^8-1;
adc3=adc3raw/2^8-1;
adc4=(adc4raw/2^5)-10;

time=[0:datasize-1]*deltat;

set(0,'DefaultAxesFontName','times')
set(0,'DefaultAxesFontSize',14)
set(0,'DefaultTextFontName','times')
figure(1);
plot(time,adc1,'b','linewidth',2);
hold on;
plot(time,adc2,'g','linewidth',2);
hold off;
% axis([0 6 0 10])
xlabel('Time')
ylabel('Magnitude')
grid on

figure(2);
plot(time,adc3,'m','linewidth',2);
xlabel('Time')
ylabel('Magnitude')
grid on
```

APPENDIX B. LOW PASS FILTER MATLAB® CODE

```
% Compute and display Fourier series coefficients
% LT Sean McConnon
% xVec must have dimensions of 1 X T/dt

function [ckVec, fVec] = LPF(xVec, T, k_max, dt)

if nargin < 4, dt = .01;
end

kVec = -k_max:k_max;
tVec = 1:dt:T;

fVec = kVec'/T;                                  % fourier frequencies

fourierMat = exp(1i*2.0*pi*(fVec*tVec));

ckVec = (1/T) * conj(fourierMat) * xVec.* dt;     % fourier
coeffecients

figure
stem(fVec,abs(ckVec))             %spectrum plot
title('Spectrum Plot')
fourierSum = ckVec.'*fourierMat;  % fourierSum is signal representation
using fourier series

%figure
%plot(tVec,xVec,'-r')
%plot(tVec,fourierSum,'-b')
plot(tVec,xVec,'-y',tVec,fourierSum,'-.b')           % plot input
signal and signal generated from function inputs

axis('auto')
title('Signal')
h = legend('Input Signal','Represented Signal',2);
set(h,'Interpreter','none')

hold off
end
```

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